DIGITAL COMMUNICATION

LABORATORY MANUAL (ECE - 417)

IV/IV ECE SEM - I

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ANIL NEERUKONDA INSTITUTE OF TECHNOLOGY & SCIENCES (A)
(Affiliated to AU, Approved by AICTE & Accredited by NBA) Sangivalasa-
531 162, Visakhapatnam District, Phone: 08933-225083/84/87

VISION OF INSTITUTE

ANITS envisions to emerge as a world-class technical institution whose products represent a good blend of technological excellence and the best of human values.

MISSION OF INSTITUTE

To train young men and women into competent and confident engineers with excellent communicational skills, to face the challenges of future technology changes, by imparting holistic technical education using the best of infrastructure, outstanding technical and teaching expertise and an exemplary work culture, besides molding them into good citizens.

VISION OF DEPARTMENT

To become a centre of excellence in Education and Research and produce high quality engineers in the field of Electronics and Communication Engineering toface the challenges of future technology changes.

MISSION OF DEPARTMENT

To achieve vision department will

- Transform students into valuable resources for industry and society by imparting contemporary technical education.
- Develop interpersonal skills and leadership qualities among students by creating an ambience of academic integrity to participate in various professional activities.
- Create a suitable academic environment to promote research attitude among students.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1: Graduates excel in their career in the domains of Electronics, Communication and Information Technology

PEO2: Graduates will practice professional ethics and excel in professional career through interpersonal skills and leadership qualities

PEO3: Graduates demonstrate passion for competence in higher education, research and participate in various professional activities

PROGRAM OUTCOMES (POs)

PO-1 **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization for the solution of complex engineering problems.

PO-2 **Problem analysis:** Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO-3 **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs.

PO-4 **Conduct investigations of complex problems:** An ability to design and conduct scientific and engineering experiments, as well as to analyze and interpret data to provide valid conclusions

PO-5 **Modern tool usage:** Ability to apply appropriate techniques, modern engineering and IT tools, to engineering problems.

PO-6 **The engineer and society:** An ability to apply reasoning to assess societal, safety, health and cultural issues and the consequent responsibilities relevant to the professional engineering practice

PO-7 **Environment and sustainability:** An ability to understand the impact of professional engineering solutions in societal and environmental contexts

PO-8 **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO-9 **Individual and team work:** Ability to function effectively as an individual, and as a member or leader in a team, and in multidisciplinary tasks.

PO-10 **Communication:** Ability to communicate effectively on engineering activities with the engineering community such as, being able to comprehend and write effective reports and design documentation, make effective presentations.

PO-11 **Project management and finance:** An ability to apply knowledge, skills, tools, and techniques to project activities to meet the project requirements with the aim of managing project resources properly and achieving the project's objectives.

PO-12 **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSOs)

PSO1: Implement Signal & Image Processing techniques using modern tools.

PSO2: Design and analyze Communication systems using emerging techniques.

PSO3: Solve real time problems with expertise in Embedded Systems.

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DIGITAL COMMUNICATION LABORATORY

ECE 417	**Credits:2**
Instruction: 3 Practical	Sessional Marks:50
End Exam: 3 Hours	End Exam Marks:50

Prerequisites: Communication Systems Engineering, Digital Communications,Signals and Systems.

Course Outcomes:

At the end of the course, the students will be able to:

1. Evaluate the performance of PCM, DPCM and Delta modulation schemes.
2. Implement different digital modulation schemes like FSK, PSK, and DPSK.
3. Analyze source/channel encoding & decoding methods.
4. Simulate Pulse Digital Modulation & demodulation using MATLAB.
5. Simulate digital communication techniques like ASK, FSK & PSK.

CO-PO-PSO Mapping:

		PO												PSO			PIs
		1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**	
CO	**1**	2		2	2				1	1	1				3		PI: 1,3,1,1.4.1,3.1.1,3.1.6, 3.2.1, 4.1.1, 4.1.3,4.3.1,8.1.1,9.1.1,9.2.2,10.1.1,10.1.2
	2	3		3	2				1	1	1				3		PI: 1.1.1,1.3.1,1.4.1, 3.1.1,3.1.6, 3.2.1,3.2.3,3.3.1,3.4.1, 4.1.1, 4.1.3,4.3.1,8.1.1,9.2.1,9.2.2, 10.1.1,10.1.2
	3	2		3	3				1	1	1				3		PI: 1.3.3,1.4.1, 3.1.1,3.1.6, 3.2.1, 3.2.3,3.3.1,3.4.1,4.1.1, 4.1.3,4.1.4,4.2.1,4.3.1,8.1.1,9.2.1,9.2.2, 10.1.1,10.1.2
	4	2		2	2	3			1	1	1				3		PI: 1.3.1,1.4.1, 3.1.1,3.1.6, 3.2.1, 4.1.1, 4.1.3,4.3.1,5.1.1,5.1.2,5.2.2,8.1.1,9.2.1,9. 2.2, 10.1.1, 10.1.2
	5	2		2	2	3			1	1	1				3		PI: 1.3.1,1.4.1,3.1.1, 3.1.6, 3.2.1, 4.1.1, 4.1.3,4.3.1,5.1.15.1.2,5.2.2,,8.1.1,9.2.1,9. 2.2, 10.1.1, 10.1.2

Justification of Mapping of Course Outcomes with Program Outcomes:

For PO1 – PO5	
If percentage of PIs related to CO >40%	Level 3
If percentage of PIs related to CO 21% to 40%	Level 2
If percentage of PIs related to CO ≤20%	Level 1
For PO6 – PO12	
If percentage of PIs related to CO >51%	Level 2
If percentage of PIs related to CO ≤50%	Level 1

CO	PO											
	1	2	3	4	5	6	7	8	9	10	11	12
CO1	40%		23%	30%				33%	28%	28%		
CO2	60%		46%	30%				33%	28%	28%		
CO3	40%		46%	50%				33%	28%	28%		
CO4	40%		23%	30%	50%			33%	28%	28%		
CO5	40%		23%	30%	50%			33%	28%	28%		

CO1-CO5	Students are expected to P1.1.1 Apply mathematical techniques such as Probability theory and Random process, Fourier series, Fourier Transform, Laplace Transform, and Z-Transform to solve problems. P1.3.1 Apply fundamental engineering concepts to solve engineering problems P1.4.1 Apply Electronics and Communication engineering concepts to solve engineering problems. P3.1.1 Recognize that need analysis is key to good problem definition P3.1.6 Determine design objectives, functional requirements and arrive at specifications P3.2.1 Apply formal idea generation tools to develop multiple engineering design solutions P3.2.3 Identify suitable criteria forthe evaluation of alternate design solutions P3.3.1 Apply formal decision-making tools to select optimal engineering design solutions for further development P3.4.1 Refine a conceptual design into a detailed design within the existing constraints (of the resources) P4.1.1 Define a problem,its scope and importance for purposes of investigation P4.1.3 Apply appropriate instrumentation and/or software tools to make measurements of physical quantities P4.1.4 Establish a relationship between measured data and underlying physical principles. P4.2.1 Design and develop an experimental approach, specify appropriate equipment and procedures P4.3.1 Use appropriate procedures, tools and techniques to conduct experiments and collect data P5.1.1 Identify modern engineering tools and techniques and resources for engineering activities. P5.1.2 Create/adapt/modify/extend tools and techniques to solve engineering problems P5.2.2 Demonstrate proficiency in using discipline-specific tools P8.1.1 Identify situations of unethical professional conduct and propose ethical alternatives P9.1.1 Recognize a variety of working and learning preferences; appreciate the value of diversity on a team P9.2.2 Treat other team members respectfully P10.1.1 Read, understandandinterprettechnicalandnon-technicalinformation. P10.1.2 Produce clear, well-constructed, and well-supported written engineering documents
Justification of Mapping of Course Outcomes with Program Specific Outcomes:	
CO1-CO3	Students are expected to use Pulse Digital Modulation, Digital modulation & channel coding techniques in Communication systems design. Hence CO1-CO3 are mapped with PSO2
CO4-CO5	Students are expected to use MATLAB Programming language for the given specification in Communication systems. Hence CO4-CO5 are mapped with PSO2.

LIST OF EXPERIMENTS

A student has to perform minimum of 10 experiments.

ABOUT DIGITAL COMMUNICATION LABORATORY

In DC lab students will be able to understand the basic theories of digital communication system, working of digital modulators and de modulators, Time division multiplexing system. With this knowledge of hardware & simulation students can design basic digital systems to solve a given communications problem

SCHEME OF EVALUATION

Total marks for each student to evaluate in lab: 100 marks

Out of 100 marks:

1. **External exam Evaluation : 50 marks**
2. **Internal Evaluation : 50 marks**
   - i. **Internal exam : 25 marks**
   - ii. **Evaluation in lab : 25 marks**

SNO.	**Student Continuous evaluation: Max.Marks:25M**	**Internal exam Max Marks: 25M**	**External Exam:50M**
1.	Student performance during every lab session / Observation book: 10M 1. Observation & performance: 5M 2. Viva-voce: 5M	Internal exam Max Marks: **25M** 1. Procedure:5M 2. Circuit/Block diagrams/ MATLAB program:5M 3. Graphs/plots: 5M 4. Result & observations: 5M 5. Viva-voce: 5M	End Exam Marks: 50 1. Procedure: 10M 2. Circuit/Block diagrams/ MATLAB Program:10M 3. Observations / Tabular forms/:10M 4. Results: 5M 5. Graphs/plots:5M 6. Viva-voce:10M
2.	Record marks (Avg. of all experiments) :10M 1. Aim, Apparatus, Theory and Procedure: 3M 2. Circuit/Block diagrams/ MATLAB program, Model Graph, Observations: 3M 3. Result:2M 4. Graphs/plots: 2M		
3.	Attendance:**5Marks** Depends on percentage of LAB attendance 66% to 100% 1. >90= 5M 2. >80-90=4M 3. >75-80=3M 4. >=66-75=2M 5. <66% =0M		

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RUBRICS
DC Laboratory

S.No	Performance Indicator	Excellent >80% to ≤ 100%	Good >60% to ≤ 80%	Average >40% to ≤ 60%	Poor performance ≤ 40%
1.	An ability to identify, formulate and solve Communication System problems with communication engineering knowledge and to conduct experiments as well as design, analyse and interpret data as an **individual or with a team.** An Ability to use the technical skills and modern simulation tools (**5M)** **(PO1, PO3, PO4, PO5 & PO9)**	Able to apply the concepts of electronics and communication engineering to solve the given problems. Able to Develop a design Strategy, analyze and decompose work into sub tasks. Able to conduct the experiment using the modern simulation tools and/or available hardware resource effectively and able to correlate the theoretical concepts with the concerned lab results with appropriate reasons.	Shows nearly complete understanding of concepts of communication engineering in problem solving. Able to Develop a design Strategy, analyze and decompose work into sub tasks with the guidance. Knowledge on modern simulation tool/available hardware resource usage is less and there are minor problem with the implementation part and able to correlate the theoretical concepts with the concerned lab results with some difficulties.	Does not understand the concept of Communication engineering for solving the given problems. Uses a design strategy with Guidance and not able to analyze and decompose work into sub tasks. Unable to use the modern simulation tool/available hardware to produce desired output and not able to correlate the theoretical concepts with the concerned lab results.	Poor knowledge on communication engineering concept. Unable to Develop a design Strategy. Unable to handling of hardware/software for producing desired results.
2.	An ability to communicate effectively when employing **oral communications**. **(Based on viva) (5M). (PO10)**	Able to **describe** the purpose of doing experiment, its scope, and related theoretical concept effectively.	Presents key elements of oral presentation on purpose of doing experiment and its scope and few desired information is missing.	Less knowledge on purpose of doing experiments and its scope. Need improvement in effective communication.	Unable to describe the purpose of doing experiment and relevant theoretical information clearly.
3.	An ability to communicate effectively when employing **written Communications** by following the ethical principle of report writing. **(10M) (PO8, PO10)**	Report is well organized with very good professional writing skills and followed the **professional code of ethics.** The report contains all the desired information related to the experiment.	Report is well organized with the professional code of ethics but very few desired information's are missing.	Report is somewhat organized with missing of some useful information and unable to apply the professional code of ethics. Need improvement in the report writing.	Report contains many errors and inadequate information.

LIST OF MAJOR EQUIPMENT IN COMMUNICATION SYSTEMS ENGINEERING LABORATORY

SL.NO	NAME OF THE EQUIPMENT	MAKE	QUANTITY
1.	50 MHZ DIGITAL STORAGE OSCILLOSCOPE	TEKTRONICS	12
2.	0-30V REGULATED POWER SUPPLY	ITL /FALCON/APLAB	14
3.	1MHZ FUNCTION GENERATOR	APLAB	07
4.	20 MHZ DUAL TRACE OSCILLOSCOPE	CADO	04
5.	3KVA ONLINE UPS	MEGAPOWER	01
6.	BLOCK CODE ENCODER&DECODER	SCIENTECH	02
7.	CONVOLUTION CODE ENCODER&DECODER	SCIENTECH	02
8.	ACL-AMPLITUDE MODULATION&DEMODULATION	AKADEMIKA LAB SOLUTIONS	02
9.	PL-DSP TRAINER KIT	AKADEMIKA LAB SOLUTIONS	02
10.	PERSONAL COMPUTER SYSTEM	HCL	06
11.	SPECTRUM ANALYZER	AGILENT TECHNOLOGIES PVT.LIMITED	01

TOTAL EXPENDITURE OF THE LABORATORY (including consumables) : Rs 27,79,409.37/-

Do's

1. Be punctual and regular to the laboratory.
2. Maintain Discipline all the time and obey the instructions.
3. Read and understand how to carry out an experiment thoroughly before coming to the laboratory.
4. Check the connections properly before turning ON the circuit.
5. Turn OFF the circuit immediately if you see any component heating.
6. Dismount all the components and wires before returning the kit.
7. Report any broken plugs/apparatus or exposed electrical wires to the faculty member/laboratory technician immediately.
8. Shut down the systems properly

Dont's

1. Don't touch live electric wires.
2. Don't turn ON the circuit unless it is completed.
3. Avoid making loose connections.
4. Do not remove anything from the kits/experimental set up without permission.
5. Do not handle any equipment without reading the instructions/Instruction manuals
6. Don't leave the lab without permission.

1.PULSE CODE MODULATION

AIM

1. To Generate Pulse Code Modulation and Demodulation
2. To Study the effect on the variation of the Amplitude of the Modulating Signal.
3. To Study the variation of Sampling frequency on the output Demodulation signal and to prove the Nyquist Sampling Theorem.

INTRODUCTION & THEORY

In analog communication systems, the limitation is that once noise is introduced at any place along the channel, we are 'stuck up' with it. To overcome such a situation, a process known as 'Quantisation' is introduced in which the analog signal is approximated to the nearest whole number of small steps of each size S. This process of quantisation is during every sampling interval. Sampling of the Analog signal however is done at a rate keeping in view of the Nyquist criterion.

In the process of quantisation approximation is made to make the number of steps a whole number resulting in an approximation error of ± S/2 . This approximation noise or quantisation noise is reproduced in the demodulation and is inseparable from the original signal.

The quantised steps represented as a binary number (of Pulses) is transmitted to the Receiver. This whole process of sampling. Quantisation and conversion into a Binary code is known as Pulse Code Modulation (PCM) . Thus in PCM the code represented at a particular time slot (sampling period) is representative of the instantaneous amplitude of the Analog signal.

At the receiving end, the pulses which are accompanied by noise or rounded off due to channel bandwidth limitation are reconstructed and clock frequency is derived from it using PLL techniques . The reconstructed signal retimed with the regenerated clock.

The resulting digital signal is converted into Analog form using D/A Converter and Low Pass Filter.

The PCM signal being in digital from transmission through low quality channels (with low SNR is possible without any loss of quality.

However the band width required for PCM signals increases largely on the basis of Sampling frequency and number of clock pulses per sample.

The Digital Telephony, Digital Video etc. are a result of PCM techniques being used extensively for better quality in combating noise in transmission.

HARDWARE DESCRIPTION :

SIGANL SOURCES

1. AF Signal Generator : 200Hz - 2KHz
2. Clock Generator
   - Conversion Clock : 68KHz - 300 KHz
   - Data Clock : 32KHz - 150 KHz
   - Byte Clock : Data Clock
   - Sampling Clock : 8.75KHz - 19KHz
3. Variable DC Source : +2.5V - -2.5V

PCM MODULATOR

4. Analog Sample and Hold.
5. 8 Bit Analog to Digital converter.
6. Parallel to Serial converter.

PCM DEMODULATOR

7. Serial to Parallel converter.
8. 8 Bit Latch.
9. 8 Bit Digital to Analog converter with Current output.
10. Current to Voltage converter
11. Low Pass Filter(3.4KHz cut off).

CIRCUIT DESCRIPTION :

1. AF SIGNAL GENERATOR

The 8038 IC is a versatile Function Generator IC which generates Sine ,Square and Triangle Waveforms. The frequency is 200Hz to 2KHz which is generated by an independent capacitor 0.01μF. The Sine wave Symmetry is adjustable by means of a preset 10KΩ connected between pins 4 and 5 of the IC 8038. The 100KΩ potentiometer adjusts the frequency of oscillations . The Sine wave output of 8038 at pin 2 is buffered by two Op Amps of TL084. The first Op Amp gives a unity non inverting gain while the latter gives an inverting gain of unity. The final output is taken through a 1KΩ potentiometer to adjust to required amplitude.

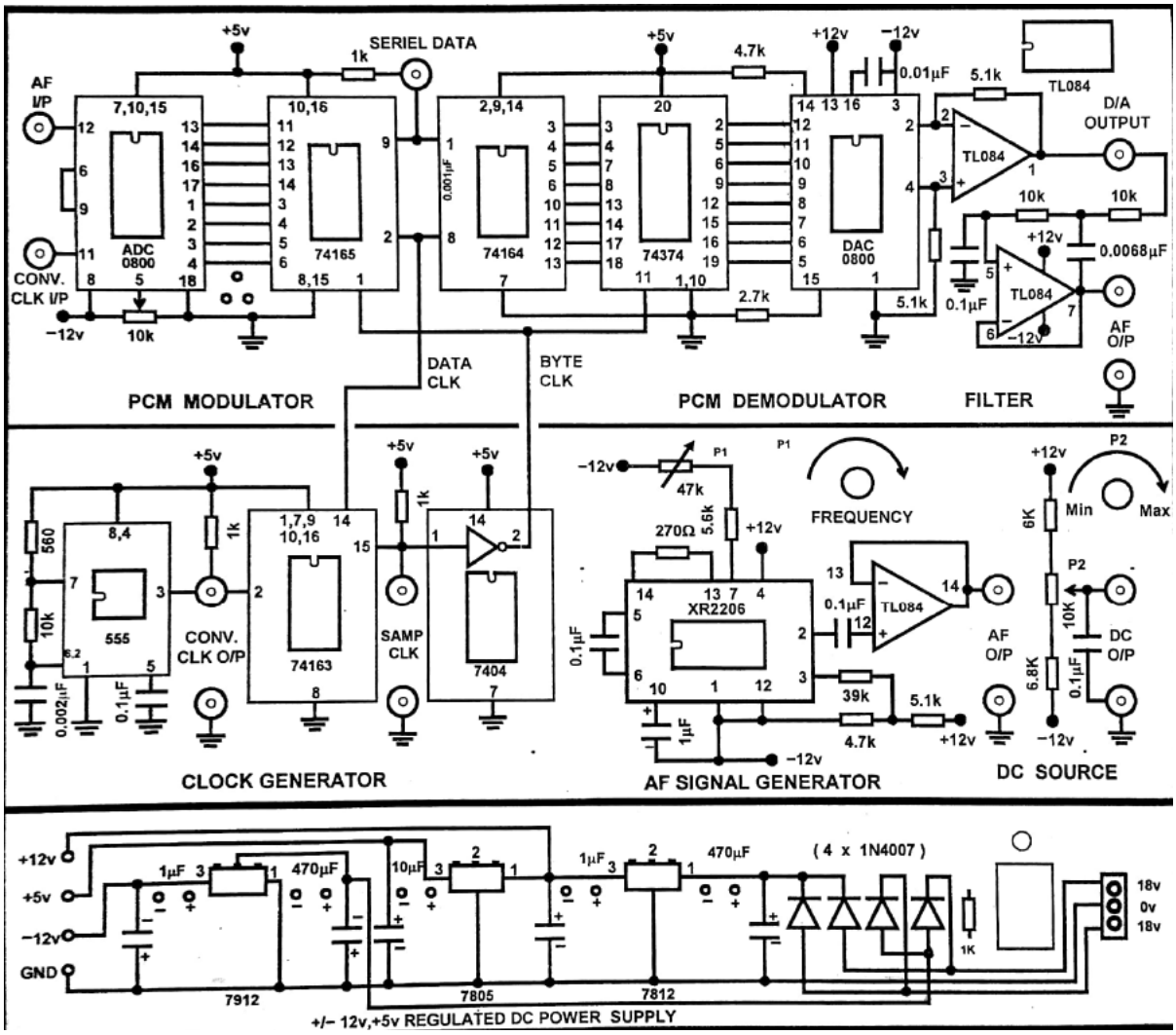
Additionally a DC signal variable from 0V to ±2.5V DC is provided through a potentiometer P_3 for studying steady-state conditions.

2. CLOCK GENERATOR

The circuit is designed around the popular timer IC 555 operated in Astable mode.Using a timing capacitor of 470pF and a potentiometer P_4 which is 22KΩ the required variation of 68KHz to 300KHz Square wave output is generated.

This output is divided by Flip - Flop in 74163 IC to give frequencies from 34Hz to 150KHz. This is used as a Bit clock in PCM.

Circuit Diagram:



3. SAMPLE PULSE GENERATOR

The output of Bit clock generator I.e 34KHz to 150KHz is given to a series of 3 Flip-Flops(divided by 8) to give frequencies from 8.75KHz to 19KHz.

4.ANALOG SAMPLE AND HOLD

The Analog Signal from the AF Signal Generator or Variable DC Source is buffered by a unity gain non inverting amplifier connected to the Sampling gate. The Buffer Amplifier is used to give a low output impedance so that the Hold capacitor gets charged instantaneously. CD4052 Analog Switch is used as a Sampling gate.

The gate is closed during the 'ON' time (+5V) of the Sampling Pulse and open (0V) during its 'OFF' time.During the 'OFF' time the capacitor holds the output level of the signal.

5. ANALOG TO DIGITAL CONVERTER

ADC 0800 is an 8 Bit Analog to Digital converter using successive approximation method. A high frequency Conversion Clock converts the Analog Signal into a Parallel Digital Word . For the Input range varies from –2.5V to +2.5V , the output varies monotonically from 00 to FF I.e -126 to +126 levels(I.e total 256 levels).

6. PARALLEL TO SERIEL CONVERTER

The Parallel Digital Word from the ADC is transferred by Parallel Load Clock in a Parallel to Serial Converter 74165. A Serial Shift Clock which is 8 times higher than Parallel Load Clock shifts the Bits in the 8 Bit Word serially. This is the Serial PCM Data.

7. SERIAL TO PARALLEL CONVERTER

At the Demodulating end the received Serial data is converted back into a Parallel Word using Serial to Parallel converter 74164. The same Serial Shift Clock helps in shifting the bits.

8. 8 BIT LATCH

The Parallel Word available at the Serial to Parallel Converter cited above is transferred into 8 Bit Word in a 8 Bit Latch (74374) using Parallel Load Clock. The 8Bit Word is held till the next word arrives after the next Sampling Pulse.

9. DIGITAL TO ANALOG CONVERTER

The DAC 0800 is a 8 Bit Digital to Analog Converter. The output is proportional (current form) to the Bit Code present at the 8 data input. An Op Amp is used to convert the output current to voltage. This output voltage is in the form of a stepped waveform similar to the S & H waveform except for the quantisation error.

10. LOW PASS FILTER

The stepped Analog waveform from the DAC is filtered and smoothed by a Low Pass Filter with 3.4KHz cut off frequency . This is a replica / reproduced / demodulated Analog Signal.xx

EQUIPMENT REQUIRED

1. FUTURE TECH Pulse Code Modulation and Demodulation Trainer.
2. Oscilloscope - 20 MHz , Dual Trace.
3. Set of Patch Chords (1set).
4. User Manual.

EXPERIMENTAL PROCEDURE

I . STUDY OF THE PULSE CODE MODULATION AND DEMODULATION

1a Connect the AC Adaptor to the mains and the other side to the Experimental Trainer. Switch 'ON' the power.

1b Observe the 'Analog output' signal on the Oscilloscope .Familiarize its variation of amplitude and frequency by means of potentiometers P_1 and P_2.

2. Set the frequency about 1KHz and its amplitude to ± 2.5V (i.e 5V p-p).

3. Connect the 'Analog output' to the ' Analog input 'of the Sample and Hold circuit using a 2mm patch chord.

4. Observe the output of 555 IC timer 'Conversion Clock output ' . Observe the variation of frequency by means of Potentiometer P_4

5. Simultaneously observe the ' Parallel Load Clock output ' (I.e divided by 16) on the other channel of the Oscilloscope

6. Adjust the frequency of 'Sampling Clock' so that its is about 8KHz and connect it to Sample and Hold circuit using a 2mm patch chord.

7. Observe the Analog output Signal and Sample and Hold output on both the channels of the Oscilloscope.

8. During the 'ON' period of Sampling Pulse the 'Analog Signal' is sampled and during its 'OFF' period the Analog Signal' value is held.Vary the Analog frequency on either side of the set value and observe the S&H output.

9. Connect S&H output to the ADC 'S&H input' and the 555 IC 'Conv Clock output' to ADC 'Conv Clock input'. The ADC 0800 successive approximation 8 Bit Analog to Digital Converter. The 8 successive pulses convert the Analog input into 8 Bits which appear in Parallel format. This can be observed on the LEDs provided after the ADC.

10. Observe the PCM output (Serial Shift Data) on CH1 and Sample Clock on CH2 of the Oscilloscope.

11. The PCM Serial output is already connected internally to PCM Demodulator input.

12. The Serial Shift Clock and Parallel Load Clock to the Demodulator are also connected internally.

13. Observe the output of the DAC of the amplifier (used as I to V converter) at pin 1 of TL 084(D/A output) . The DAC output resembles the S&H signal except that it is now in quantised form.

14.Observe the output of the Low Pass Filter (3.4 KHz cut off frequency) which is replica of the input Analog Signal.

2. STUDY OF THE EFFECT OF AMPLITUDE VARIATION OF MODULATING SIGNAL

1. Observe the Analog input to PCM modulator and the output of PCM Demodulator on 2 channels of the Oscilloscope.
2. Increase the Amplitude by means of Potentiometer P_2. The Amplitude is limited to ± 2.5V p-p only. The output will be reproduced undistorted.
3. Any further increase will saturate the ADC levels and the output peaks are flattened.
4. Decrease the Amplitude . The output signal amplitude will be reduced accordingly. Since lesser levels are ther in the Sine wave at lower levels, some distortion is observed even after filtering.

3. STUDY OF SAMPLING FREQUENCY ON THE OUTPUT

The Analog Signal frequency (1KHz) and Sampling frequency (8KHz) are restored using Oscilloscope before starting this part of the experiment.

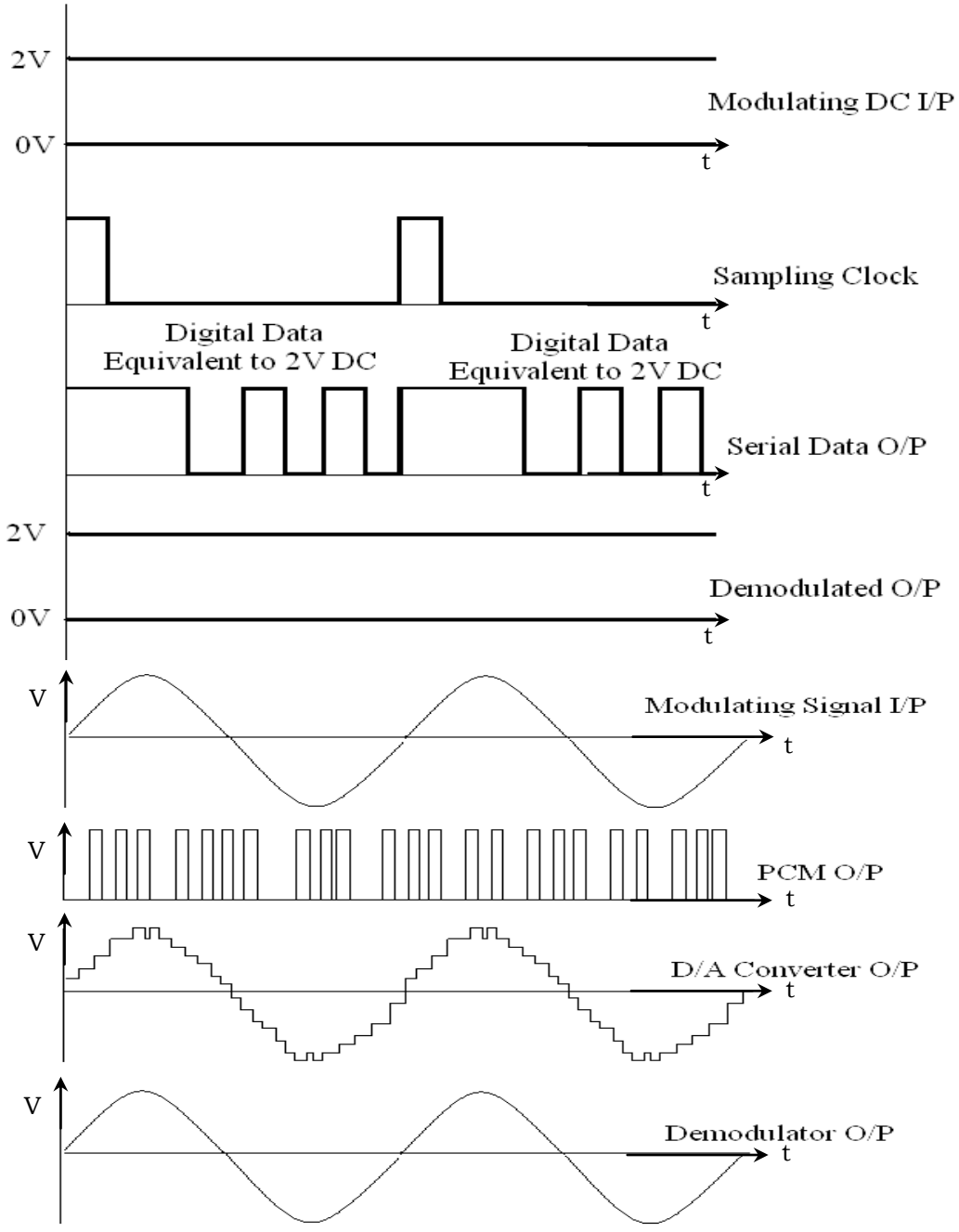
1. In each cycle of the Analog input we observe that there are about 8 Sampling Pulses. Thus the PCM Demodulated output is a true replica of input as observed on both the channels of the Oscilloscope.
2. Gradually reduce the Clock frequency using potentiometer P_4 which reduces the Sampling frequency. As the frequency decreases , the Sine wave output at one point gets so distorted that it does not resemble a Sine wave. Measure the Sampling frequency at this point. It is found that the frequency is 2KHz or even less as indicated by the Nyquist Theorem.

   Usually for better reproduction, the Sampling frequency should be much more than the Nyquist Rate.

HARDWARE SPECIFICATIONS

1. Pulse Code Modulation and Demodulation Trainer Kit.
2. Built in DC power supply ±12V, ±5V / 350mA.
3. Provided with 2mm Sockets.
4. The ICs provided on the board are TL084, 7404 , 74163 , 555 , 8038 , 74164 , 74165 , 74374 , DAC 0800 , ADC 0800 , CD 4053 .
5. Set of Patch chords Stackable 2mm - 10 Nos.
6. User Manual.

MODEL WAVEFORMS:



PRECAUTIONS:

1. Avoid loose and wrong connections.
2. Readings should be noted without parallax error.

RESULT:

Thus Pulse Code Modulation signal is generated for both AC and DC input signals and it is Demodulated.

VIVA QUESTIONS:

1. What do you mean by quantizing process?
2. What will happen when sampling rate is greater than Nyquist rate ?
3. What will happen when sampling rate is less than Nyquist rate ?
4. Find the A/D Converter output for input DC voltage of 3.6V.
5. Fig shown below shows a PCM wave in which the amplitude levels of +1 volt and -1 volt are used to represent binary symbols 1 and 0 respectively. The code word used consists of three bits. Find the sampled version of an analog signal from which this PCM wave is derived.
6. Mention some applications of PCM.
7. What is the function of Sample and Hold circuit?

2. DIFFERENTIAL PULSE CODE MODULATION & DEMODULATION

AIM

To study Differential Pulse Code Modulation & Demodulation by sending variable frequency sine wave and variable D.C signal inputs.

INTRODUCTION

Pulse Code Modulation (PCM) is different from Amplitude Modulation (AM) and Frequency Modulation (FM) because, those two are continuous forms of modulation. Pulse Code Modulation (PCM) is used to convert analog signals into binary form. In the absence of noise and distortion it is possible to completely recover a continuous analog modulated signals. But in real time they suffer from transmission distortion and noise to an appreciable extent. In the PCM system, groups of pulses or codes are transmitted which represent binary numbers corresponding to Modulating Signal Voltage levels. Recovery of the transmitter information does not depend on the height, width, or energy content of the individual pulses, but only on their presence or absence. Since it is relatively easy to recover pulses under these conditions, even in the presence of large amounts of noise and distortion, PCM systems tend to be very immuse to interference and noise. Regeneration of the pulse enroute is also relatively easy, resulting in system that produces excellent result for long-distance communication.

Differential PCM is quite similar to ordinary PCM. However, each word in this system indicates the difference in amplitude, positive or negative, between this sample and the previous sample. Thus the relative value of each sample is indicated rather than, the absolute value as in normal PCM.

The rational behind this system is that speech is redundant, to the extent that each amplitude is related to the previous amplitude, so that large variations from one sample to the next are unlikely. This being the case, it would take fewer bits to indicate the size of the amplitude change than the absolute amplitude, and so a smaller bandwidth would be required for the transmission. The differential PCM system has not found wide acceptance because complications in the encoding and decoding process appear to out weigh any advantages gained.

DPCM ENCODING

DPCM Encoding is similar to the PCM encoding, except that initial stage employs Delta Modulation after that PCM encoding is following.

The encoding process generates a binary code number corresponding to Modulating signal voltage level to be transmitted for each sampling interval. Any one of the codes like binary, ASCII etc, may be used as long as it provides a sufficient number of different symbols to represent all of the levels to be transmitted. Ordinary binary number will contain a train of ' 1 ' and '0' pulses with a total of $\log_2 N$ pulses in each number. (N is no of levels in the full range). This system is very economical to realise, because it corresponds exactly to the process of analog - to- digital (A / D) conversion.

QUANTIZATION

The first step in the PCM system is to quantize the modulating signal. The modulating signal can assume an infinite number of different levels between the two limit values which define the range of the signal. In a PCM, a coded number is transmitted for each level sampled in the modulating signal. If the exact number corresponding to the exact voltage were to be transmitted for every sample, an infinitely large number of different code symbols would be needed. Quantization has the effect of reducing this infinite number of levels to a relatively small number which can be coded without difficulty.

In the quantization process, the total range of the modulating signal is divided up into a number of small subranges. The number will depend on the nature of the modulating signals and will form as few as eight to as many as 128 levels. A number that is an integer power of two is usually chosen because of the ease of generating binary codes. A new signal is generated by producing, each sample , a voltage level corresponding to the midpoint level of the subrange in which the sample falls. Thus if a range of 0 to 5V were divided into 128, 5/128V subranges, and the signal sampled when it was 3V, the quantizer would put a voltage of 2.96V and hold that level until the next sampling time. The result is a stepped wave form which follows the counter of the original modulating signal with each step synchronised to the sampling period Fig.1 illustrate the quantization process

QUANTIZATION NOISE

The quantized staircase waveform is an approximation to the original waveform. The difference between the two waveform amounts to "noise" added to the signal by the quantizing circuit. The mean square quantization noise voltage has a value of

$$E\ 2_{nq} = \frac{S^2}{12} \qquad \text{-------(1)}$$

where S is the voltage of each step, or the subrange voltage span. As a result, the number of quantization levels must be kept high in order to keep the quantization noise below some acceptable limit, given by the power signal-to-noise ratio, which is the ratio of average noise power. For a sinusoidal signal which occupies the full range , the mean square signal voltage is

$$E\ 2_s = \frac{1}{2} E\ 2\ Peak = \frac{1}{2} \frac{(MS)^2}{2} = \frac{(MS)^2}{8} \qquad \text{-------(2)}$$

where M is the number of steps and S is step height voltage. The signal-to-noise ratio is now given by

$$\frac{\text{Signal}}{\text{Noise}} = \frac{E2_s}{E2_{nq}} = \frac{(MS)^2}{8} \times \frac{12}{S_2} = 3M^2 \qquad \text{---------(3)}$$

The number of levels M is related to the number n of bits per level by

$$M = 2^n$$

Substituting this in Eq.(3) gives, for the signal-to-noise ratio,

$$\frac{\text{Signal (S)}}{\text{Noise (N)}} = \frac{1}{2} \times 2^{2n}$$

In decibels this becomes

$$(S/N)\ dB = 10 \log \left(3 \times \frac{2}{2} \right)^{2n}$$

$$= 1.761 + 6.02n\ dB$$

$$n = 7 \text{ bits}$$

then $(S/N)dB = 1.761 \times 6.02 \times 7 = 43.9\ dB$

DECODING

The decoding process reshapes the incoming pulses and eliminates most of the transmission noise. A serial to parallel circuit passes the bits in parallel groups to a digital to analog converter (D/A) for decoding. Thus decoded signal passes through a sample and hold amplifier which maintains the pulse level for the duration of the sampling period, recreating the staircase waveform approximation of the modulating signal. A low-pass filter may be used to reduce the quantization noise.

BLOCK DIAGRAM DESCRIPTION

The block diagram of Differential Pulse Code Modulation and Demodulation is shown on front panel.

MODULATING SIGNAL

A variable sinusoidal frequency generator is provided with frequency from '100' Hz to 500 Hz. To see the actual bits that are transmitted through the communication channel.

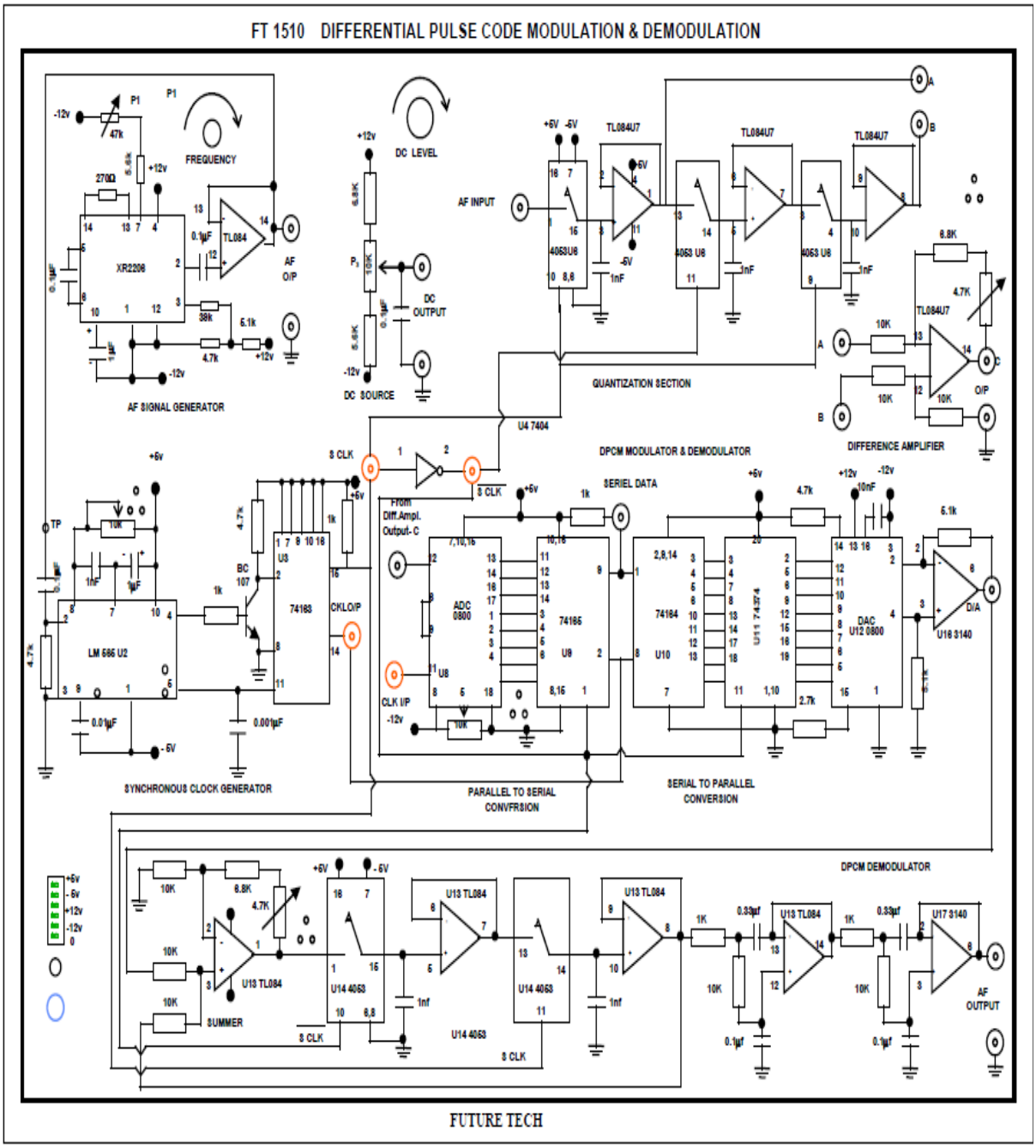
DPCM ENCODING

The modulating signal is applied to the input of Analog-to-Digital (A/D) converter which performs the two functions of quantization and encoding, producing a 8-bit binary coded number. The signal is to be transmitted i.e., modulating signal is sampled at regular intervals.

If the maximum amplitude +5V is represented by 8-bits the 1LSB corresponds to V x 1/128 = 5/128 = 39 mV and MSB represents the sign. So the values of the sampled signal at the output of Analog-to-Digital converter for Fig.2 are 0000000, 00111111, 01111111, 00111111, 00000000, 10111111, 1111111 1, 10111111, 00000000.

To transmit all the bits in channel one channel, actually it is often sent as binary number back to front by parallel to serial converter, i.e., 0000000 111111100 11111110 to make demodulating easier. A parallel to serial converter transmits the code bits in serial fashion.

Circuit Diagram:



DPCM DECODING

At the receiver end the received data will be in serial form. The serial data is converted back to parallel form by serial to parallel converter and passes the bits to a Digital-to-Analog converter for decoding which has in-built sample and hold amplifier which maintains the pulse level for the duration of the sampling period, recreating the pulse level for the duration of the sampling period, recreating the staircase wave form which is approximation of modulating signal. A low pass filter may be used to reduce the quantization noise and to yield the original modulating signal.

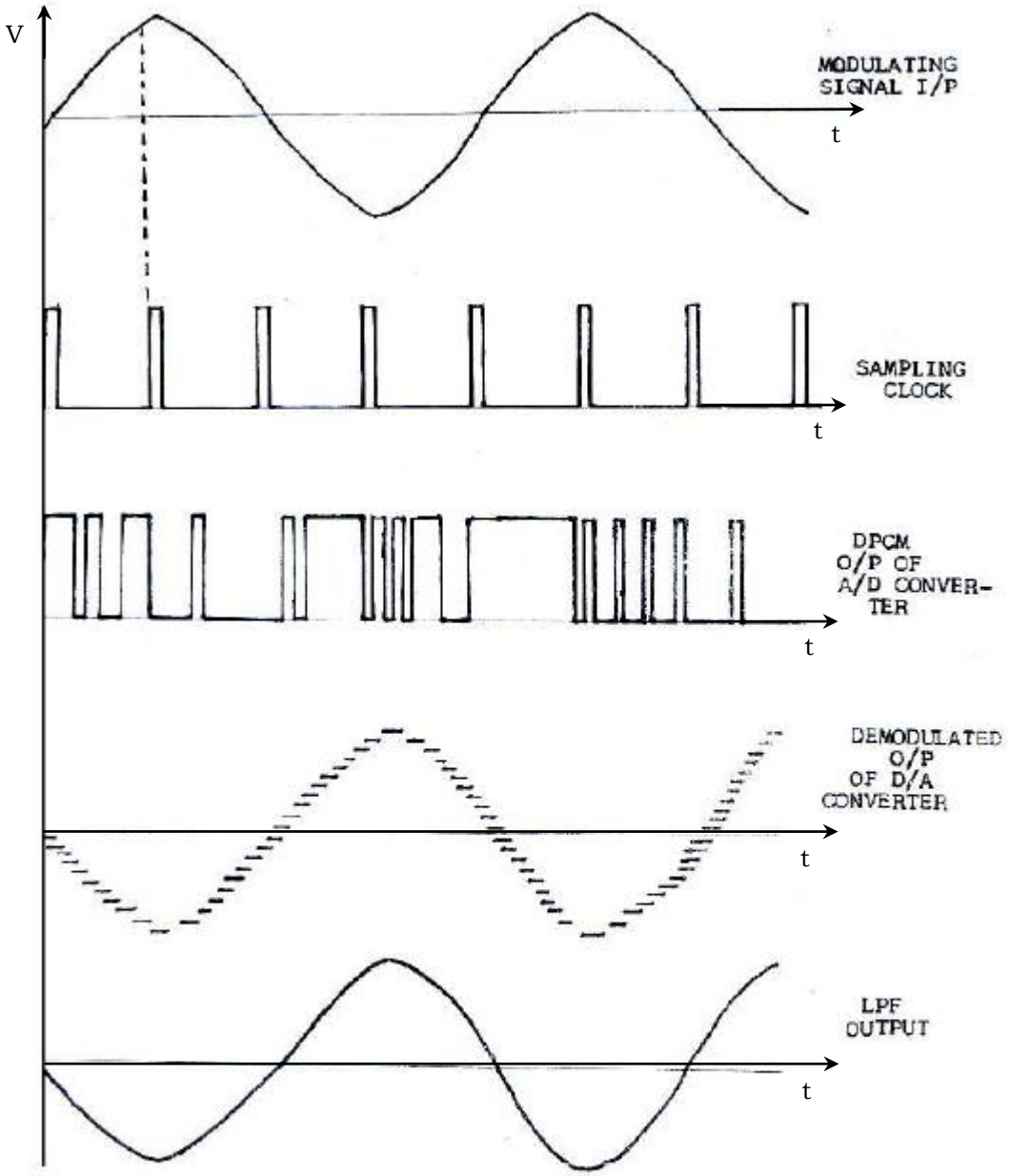
HARDWARE SPECIFICATIONS

1. AF oscillator with variable Amplitude.
2. Variable D.C Source.
3. DPCM Modulator.
4. DPCM Demodulator.

EXPERIMENTAL PROCEDURE

1. Switch 'ON' the experimental kit.
2. Connect AF output to channel 1 of oscilloscope and also connect AF oscillator output to AF input of quantization section and connect S clock and $\overline{S}$ clock to the input terminals of quantization section.
3. Observe the outputs of two different sample and hold outputs at A and B.
4. Connect A and B outputs to difference amplifier and observe the differential output C on channel 2.
5. Apply differential output C, B clk, S clock and $\overline{S}$ clock to the input terminals of DPCM modulator section.
6. Observe the DPCM output serial data and D/A output on channel 2.
7. The D/A output is given to summer and the summer output is filtered by low pass filter to give AF output.
8. Now, disconnect the differential data and apply the variable DC signal to the input of the DPCM modulator
9. By adjusting the DC voltage potentiometer we can get the DPCM output from 0000 0000 to 1111 1111

Model waveforms:



PRECAUTIONS:

1. Avoid loose and wrong connections.
2. Readings should be noted without parallax error.

RESULT:

Thus Differential Pulse Code Modulated signal is generated for given input signal and it is Demodulated.

VIVA QUESTIONS:

1. For data compression says whether ADPCM or DPCM is better. Justify.
2. What is the need for compression? Mention the types of compression.
3. List the communication standards which use DPCM.
4. Based upon the knowledge that you have gained after doing the experiment write the Functions of sample and hold circuit.
5. Name the circuit used to achieve synchronization between transmitter and receiver.

3. DELTA MODULATION

AIM

To study the Delta Modulation process by comparing the present signal with the previous signal of the given Modulating signal.

INTRODUCTION

In radio transmission, it is necessary to send audio signal (e.g. Music, speech etc.) from a broad casting station over great distances to a receiver. This communication of audio signal which does not employ any wire and is sometimes called wireless. The audio signal cannot be sent directly over the air for appreciable distance. Even if the audio signal is converted into electrical signal, the latter cannot be sent very far without employing large amount of power. The energy of a wave is directly proportional to its frequency. At audio frequencies (20Hz to 20KHz), the signal power is quite small and radiation is not practicable.

The radiation of electrical energy is practicable only at high frequencies e.g. Above 20KHz. The high frequency signals can be sent thousands of miles even with comparatively small power. Therefore, if audio signal is to be transmitted properly, some means must be devised which will permit transmission to occur at high frequencies while it simultaneously allows the carrying of audio signal . This is achieved by imposing electrical audio signal on high frequency carrier/ The resultant waves are known as modulated waves or radio waves and the process is called modulation. At the radio receiver, the audio signal is extracted from the modulated wave by the process is called modulation. At the radio receiver, the audio signal is extracted from the modulated wave by the process called demodulation. The signal is then amplified and reproduced into sound by the loudspeaker.

MODULATION

A high frequency carrier wave is used to carry the audio signal which is done by changing some characteristic of carrier wave in accordance with the signal. Under such conditions, the audio signal will be contained in the resultant wave. The process is called modulation and defined as " The process of changing some characteristic (e.g. Amplitude, Frequency or Phase) of a carrier wave in accordance with the intensity of the signal is known as Modulation".

Modulation means to "change". In modulation, some characteristic of a carrier wave is changed in accordance with the intensity (I.e. Amplitude) of the signal. The resultant wave is called modulated wave or radio wave and contains the audio signal. Therefore, modulation permits the transmission to occur at high frequency while it simultaneously allows the carrying of the audio signal.

NEED FOR MODULATION

Modulation is extremely necessary in communication system due to the following reasons.

1. PRACTICAL ANTENNA LENTH : In order to transmit a wave effectively, the length of the transmitting antenna should be approximately equal to the wavelength of the wave.

$$\text{Now} \quad \text{Wavelength} = \frac{\text{Velocity}}{\text{frequency}} = \frac{3 \times 10^8}{\text{frequency (Hz)}} \text{ meters}$$

As the audio frequencies range from 20Hz to 20KHz, therefore, if they are transmitted directly into space, the length of the transmitting antenna required would be extremely large. For instance, to radiate a frequency of 20KHz directly into space, we would need an antenna length of $3 \times 10^8 \setminus 20 \times 10^3 = 15{,}000$ meters. This is too long antenna to be constructed practically. For this reason, it is impracticable to radiate audio signal directly into space. On the other hand, if a carrier wave say of 1000KHz is used to carry the signal, we need an antenna length of 300 meters only and this size can be easily constructed.

2. OPERATING RANGE

The energy of a wave depends upon its frequency. The greater the frequency of the wave, the greater the energy possessed by it. As the audio signal frequencies are small, therefore these cannot be transmitted over large distances if radiated directly into space. The only practical solution is to modulate a high frequency carrier wave with audio signal and permit the transmission to occur at this high frequency (I.e carrier frequency).

3. WIRELESS COMMUNICATION

One desirable feature of radio transmission is that it should be carried without wires I.e. Radiated into space. At audio frequencies radiation is not practicable because the efficiency of radiation is poor. However, efficient radiation of electrical energy is possible at high frequencies. For this reason, modulation is always employed in communication systems.

INTRODUCTION

Delta Modulation is a Differential Pulse Code Modulation Technique, in which the difference signal between two successive samples is encoded into a single bit code.

Circuit Diagram:

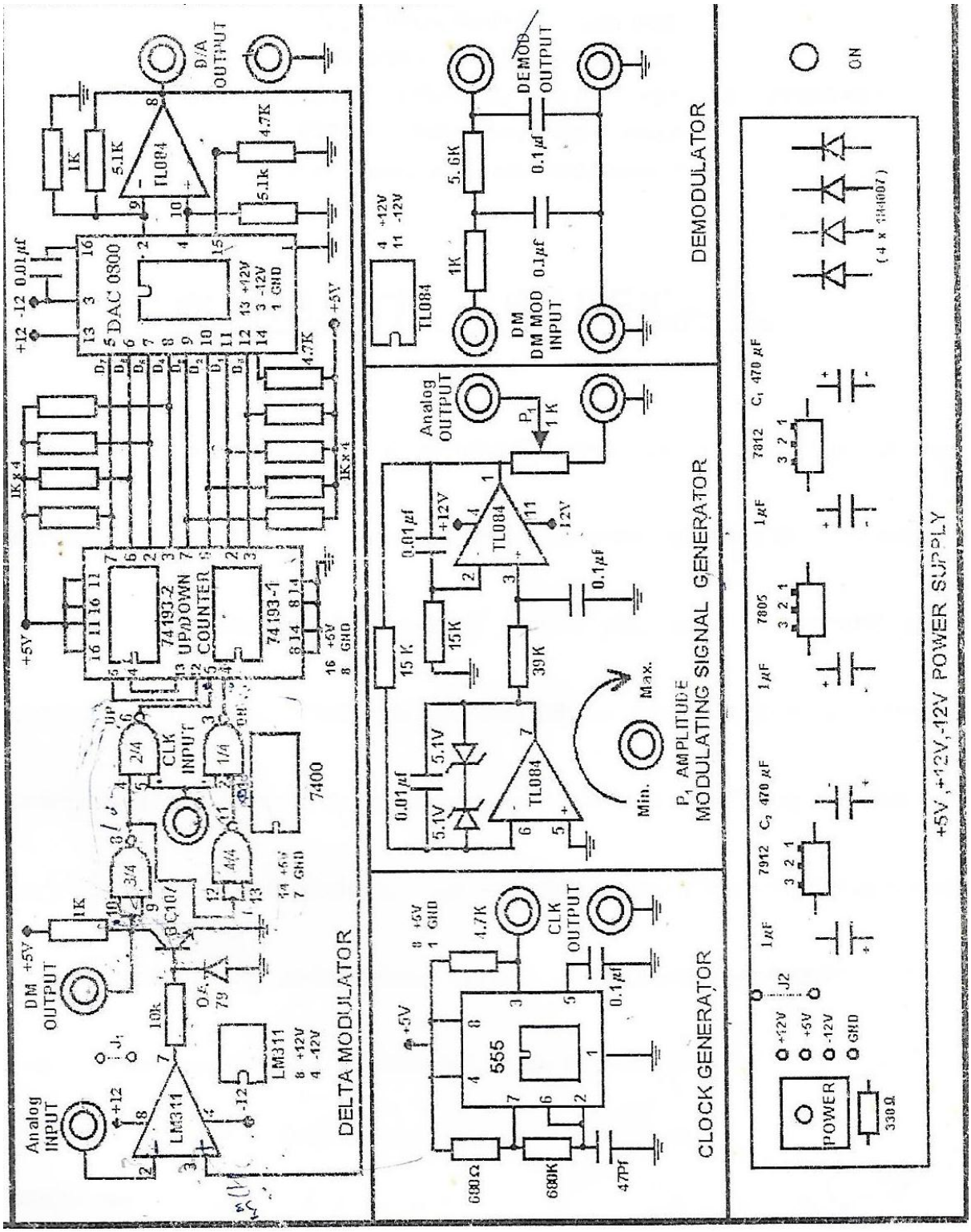


Fig-1 shows the block diagram of the Delta Modulation. This is also known as Linear Delta Modulator. The signal m(t) is the analog input signal. While r(t) is a reconstructed signal which is same as the quantised input signal with 1 bit delay. The signal r(t) tries to follow the input signal m(t) with one bit period delay.

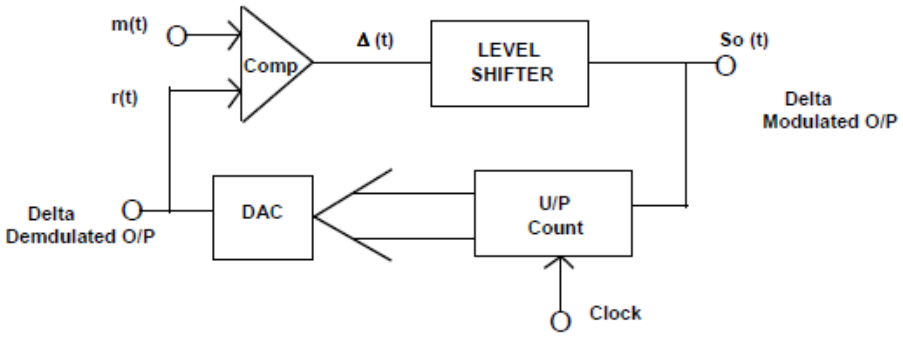


FIG - 1 BLOCK DIAGRAM OF DELTA MODULATION

THEORY

The process of encoding is as follows. The comparator compares the input signal m(t) and r(t). If m(t) > r(t) a logic 1 is generated at the output of the comparator, otherwise a logic 0 is generated.The value of logic 1 or logic 0 turmed as Δ(t) is held for the bit duration by the sample and hold current to generate So (t), the Delta Modulated Output.

This output So(t) is fed to the 8 bit binary up/down counter to control it's count direction. A logic 1 at the mode control input increases the count value by one and a logic '0' decrements the count value by one . All the 8 outputs of the counter are given to DAC to reconstruct the original signal. In essence the counter & Decoder forms the Delta Modulator in the feedback loop of the comparator. Thus, if the input signal is higher than the reconstructed signal the counter increments at each step so as to enable the DAC output to reach to the input signal values. Similarly if the input signal m(t) is lower than the reconstructed signal r(t), the counter decrements at each step, and the DAC output gets reduced to reach a value to that of m(t).

The block diagram of Delta demodulator is shown below. It works in the same way as it was in the feedback loop of the Delta modulator. The received Delta modulated signal So(t) is given to the mode control input (U/ D) of the up/ down counter. The counter is 8 bit wide and counts in binary fashion. All the 8 outputs are connected to an 8 bit DAC which gives a quantised analog signal (stepped waveform). A low pass filter is used to smooth out the steps. A buffer amplifier provides the necessary drive capability to the output signal. Thus the digital Delta modulated data is demodulated and reconstructed into an analog signal.

Although this process of Delta Modulation and Demodulation is a simple and cost effective method of coding, there will be poor approximation at starting buildup and ' hunting' at flat top signals.

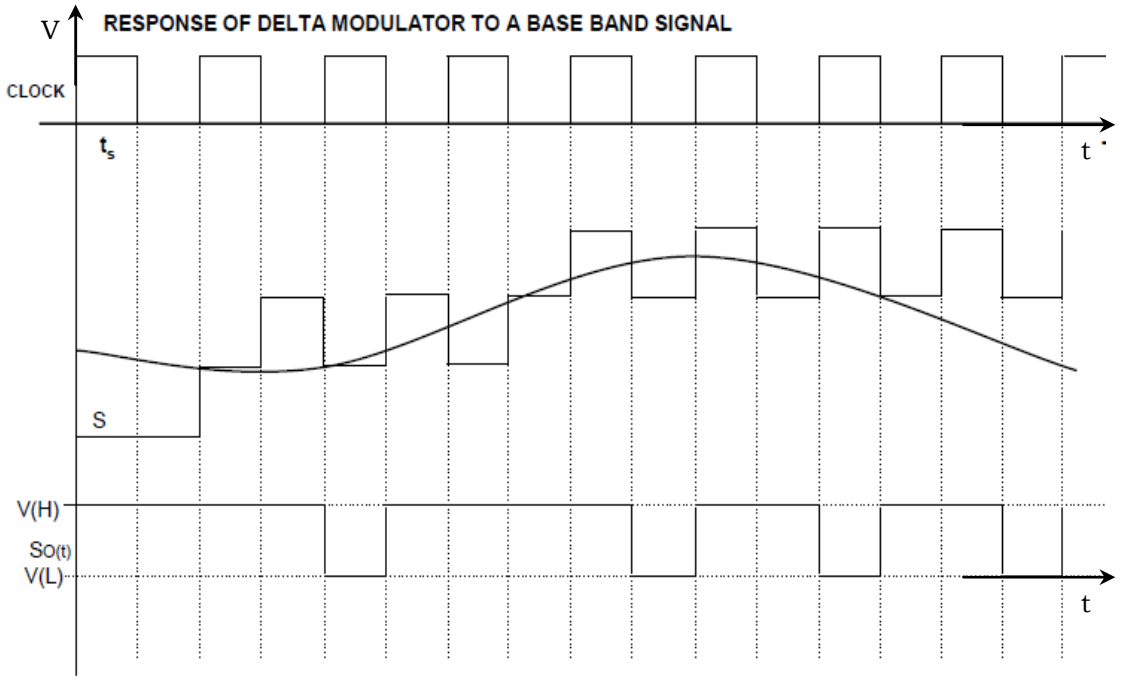


Fig - 2

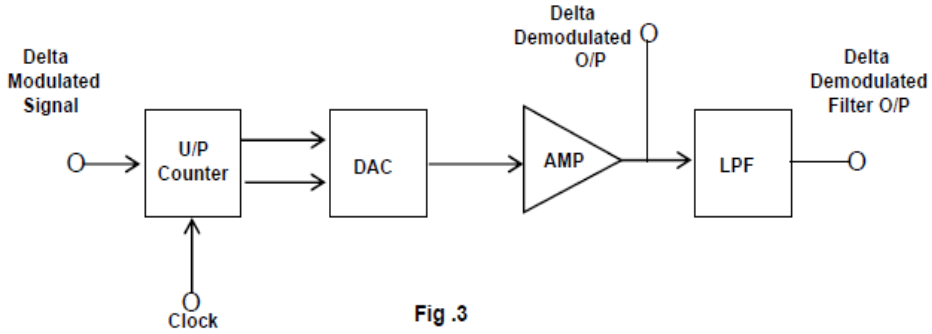


Fig .3

RESPONSE LIMITATIONS OF DELTA MODULATION

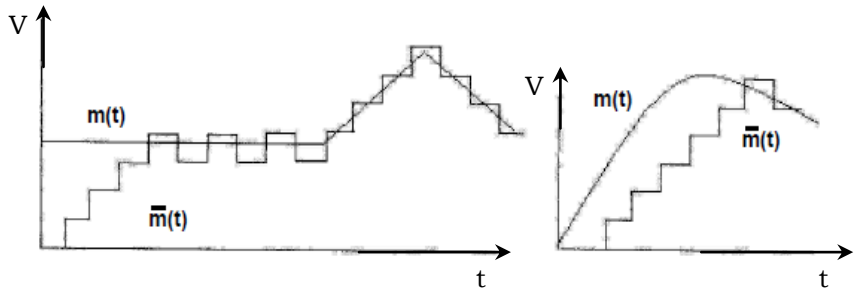


Fig .4

Another limitation in Delta Modulation is ' slope overloading;. Basically the DAC can produce a Max. signal variation of (256x 5) volts in 256 clock pulses where is the quantisation step size T_c is the clock period the max. Slope that the DAC can produce in S/ T_s volts / second which is the limiting factor where S is the step size and t_s is clock period. If the input signal slope is higher than this or in other words, if the input signal frequency is greater than the limiting value, slope overloading occurs. In such a case true reproduction of the analog signal is not possible. A sinusoidal waveform of amplitude A & frequency f has a maximum slope of 2ΔfA which occurs at zero crossing of the sine wave. If the overloading is to be avoided then the following condition should be satisfied.

$$S_f > / 2\pi fA$$

When S = quantisation step size,
f_s = sampling frequency (Bit frequency), f = Signal frequency , A = Signal Amplitude

$$f_s = \frac{2\pi fA}{S} = \frac{\pi f2A}{S}$$

When 2A = Peak to Peak Amplitude
= 256 X s = DAC Max. Amplitude
$f_s = \pi f\ 256 = 256\ \pi f$

For a signal frequency of 200Hz, the sampling frequency should be
$f_s = 256 \times \pi \times 200 = 160KHz$

HARDWARE SPECIFICATIONS

1. Delta Modulation and Demodulation Trainer.
2. Built in DC power supply + 5V / 350mA , +/- 12V / 350mA.
3. Provided with 2mm Sockets.
4. The ICs provided on the board are TL084(1No), 555 (1No), (74193 (2 Nos), DAC0800(1 No) , 7400 (1 No) , LM 311 (1 No).
5. Set of Patch chords Stackable 2mm - 6 Nos.
6. User Manual.

EXPERIMENTAL PROCEDURE

1. Connect the AC Adaptor to the mains and the other side to the Experimental Trainer.
2. Switch ON the experimental board.
3. Connect Clock Signal to the Delta Modulator circuit.
4. Connect Modulating Signal to the Modulating signal input of the Delta Modulator and observe the same on channel 1 of a Dual Trace Oscilloscope.
5. Observe the Delta Modulator output on channel II.
6. Connect this Delta Modulator output to the Demodulator.
7. Also connect the clock signal to the demodulator.
8. Observe the Demodulator output with and without RC filter on CRO.

MODEL WAVEFORMS:

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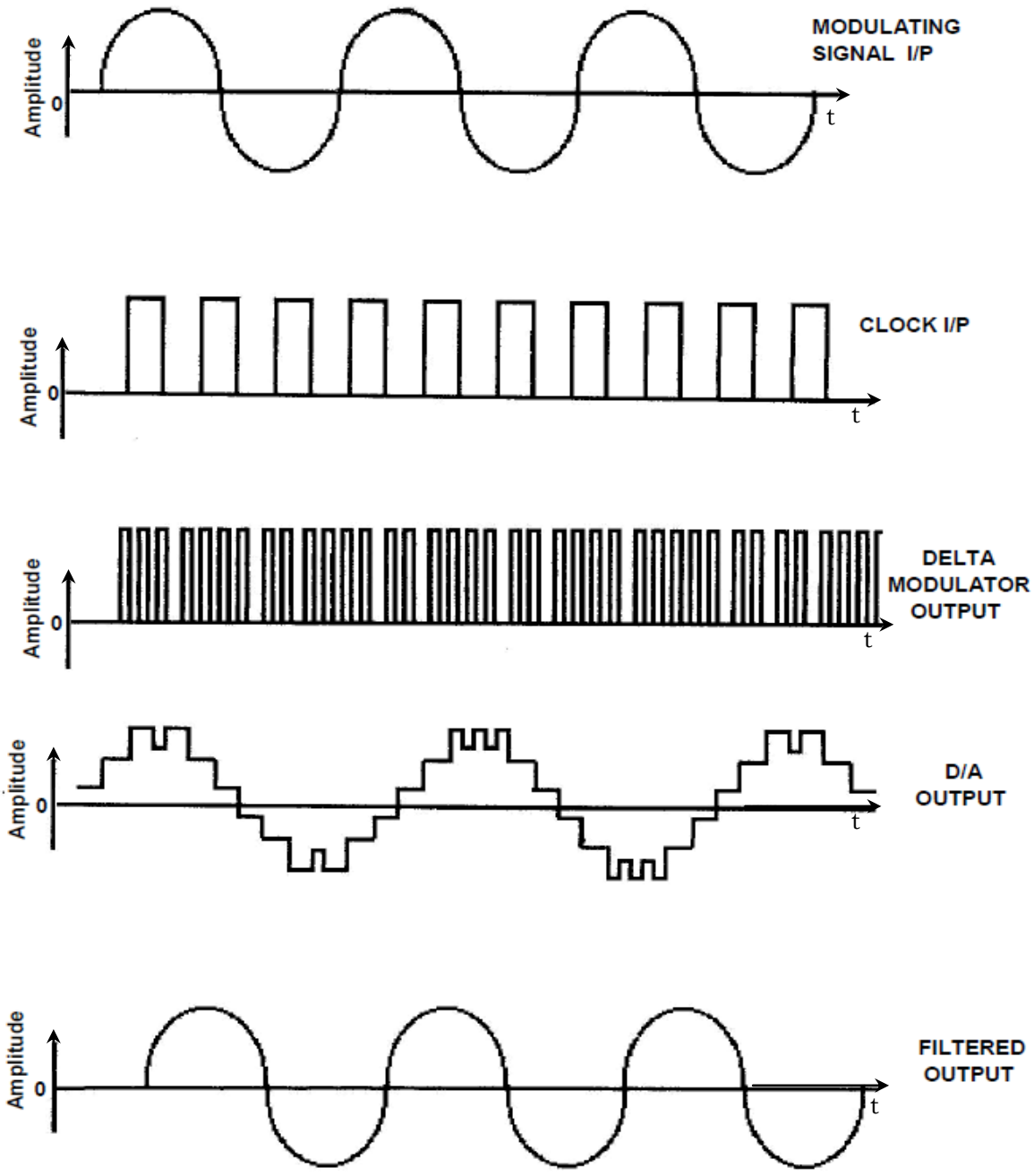


PRECAUTIONS:

1. Avoid loose and wrong connections.
2. Readings should be noted without parallax error.

RESULT:

Thus Delta Modulated signal is generated for given input signal and it is Demodulated

VIVA QUESTIONS:

1. Compare DPCM ,PCM& Delta modulation.
2. How to reduce the quantization noise that occurs in DM?
3. A band pass signal has a spectral range that extends from 20 to 82 KHz.Find the acceptable sampling frequency.
4. Find the fourier series expansion of an Impulse train.
5. Mention the applications of DM

4. PHASE SHIFT KEYING

AIM

To study the operation of PHASE SHIFT KEYING modulation and demodulation .

INTRODUCTION

Digital communications became important with the expansion of the use of computers and data processing, and have continued to develop into a major industry providing the interconnection of computer peripherals and transmission of data between distant sites. Phase Shift Keying (PSK) is a relatively new system, in which the carrier may be phase shifted by +180 degrees for a mark, and by −180 degrees for a space. PSK has a number of similarities to FSK in many aspects, as in FSK , frequency of the carrier is shifted according to the modulating square wave.

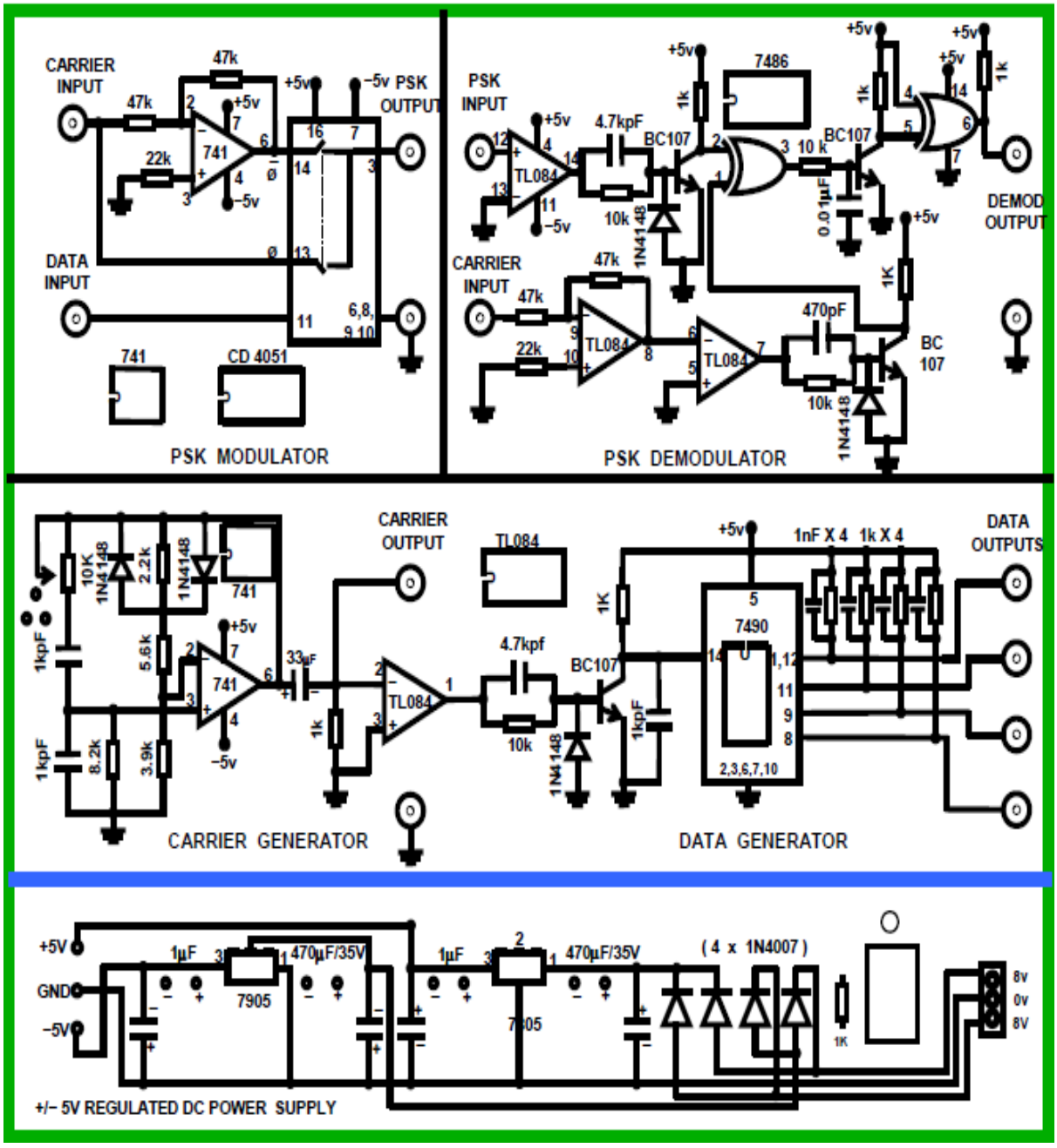
THEORY

Fig−1 shows the circuit diagram of the Phase Shift Key modulation and demodulation. In this carrier Generator is generated by a wein bridge oscillator around 28 KHz. At ± 5Vp−p sine wave using 741 IC.The sine wave is converted into square wave using TL084 in comparator mode. The transistor BC107 converts the square wave signal to TTL level. This is used as a basic bit clock or 180^0 for a mark and 0^0 for space.This square wave is used as a clock input to a decade counter (IC7490) which generates the modulating data outputs. IC CD4051 is an Analog multiplexer to which carrier is applied with and without 180° phase shift to the two multiplex inputs of the IC. Modulating data input is applied to its control input. Depending upon the level of the control signal, carrier signal applied with or without phase shift is steered the output. The 180° phase shift to the carrier signal created by an operational amplifier using 741 IC. During the demodulation, the PSK signal is converted into a + 5 volts square wave signal using a transistor and is applied to one input of an EX − OR gate. To the second input of the Logic gate, carrier signal is applied after conversion into a +5 volts signal. So the EX − OR gate output is equivalent to the modulating data signal.

Phase shift keying is a digital modulation scheme that conveys data by changing, or modulating, the phase of a reference signal (the carrier wave).

Any digital modulation scheme uses a finite number of distinct signals to represent digital data. PSK uses a finite number of phases, each assigned a unique pattern of binary bits.

Circuit Diagram:



Usually, each phase encodes an equal number of bits. Each pattern of bits forms the symbol that is represented by the particular phase. The demodulator, which is designed specifically for the symbol set used by the modulator determines the phase of the received signal and maps it back to the symbol its represents, thus recovering the original data. This requires the receiver o able to compare the phase of the received signal to a reference signal.

HARDWARE SPECIFICATIONS

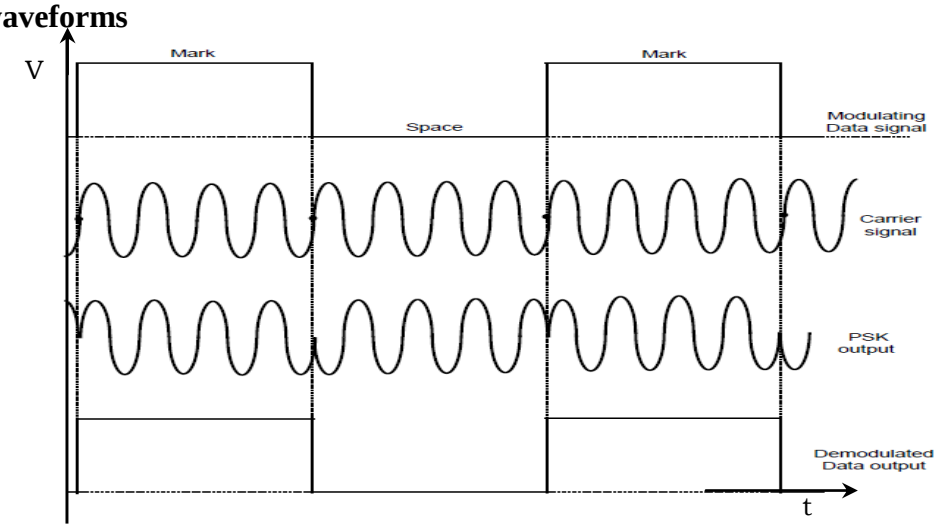
1) Panel lay out diagram with components mounted on PCB / panel.
2) Built in DC power supplies ± 5V/ 350mA.
3) Provided with 2mm sockets.
4) ICs provided on the board are 741, 7490, TL084, CD4051 & 7486.
5) Set of patch chords

   2mm Stackable patch chrods – 8 Nos.
6) user manual.

EXPERIMENTAL PROCEDURE

1. Connect the AC Adaptor to the mains and the other side to the Experimental Trainer. Switch 'ON' the power.
2. Apply the carrier signal to the input of the modulator.
3. Apply the modulating data signal to the modulator input and observe this signal on channel 1 of the CRO.
4. Observe the output of the PSK modulator on the channel 2 of the CRO.
5. Apply this PSK output to the demodulator input and also apply the carrier input.
6. Observe the demodulator output and compare it with the modulating data signal applied to the modulator input which is identical.

Model waveforms



PSK Signal Waveforms

PRECAUTIONS:

1. Avoid loose and wrong connections.
2. Readings should be noted without parallax error.

RESULT:

Thus the PSK modulation signal is generated for a given input data signal and it is demodulated.

VIVA QUESTIONS:

1. Compare FSK and PSK.
2. List the Characteristics of TL084 op-amp.
3. Compare TL084 op amp with IC 741 op amp.
4. What do we infer from constellation diagrams of various modulation schemes?

5. DIFFERENTIAL PHASE SHIFT KEYING MODULATION & DEMODULATION

AIM

To study the various steps involved in generating the differential binary signal and differential phase shift keyed signal at the modulator end and recovering the binary signal from the received DPSK signal.

INTRODUCTION

Digital communications became important with the expansion of the use of computers and data processing, and have continued to develop into a major industry providing the interconnection of computer peripherals and transmission of data between distant sites.

Phase shift keying (PSK) is a relatively a new system, in which the carrier is phase shifted by + 90 degrees for a mark, and by -90 degrees for a space.

PSK has a number of similarities to FSK in many aspects, as in FSK, frequency of the carrier is shifted according to the modulating data level.

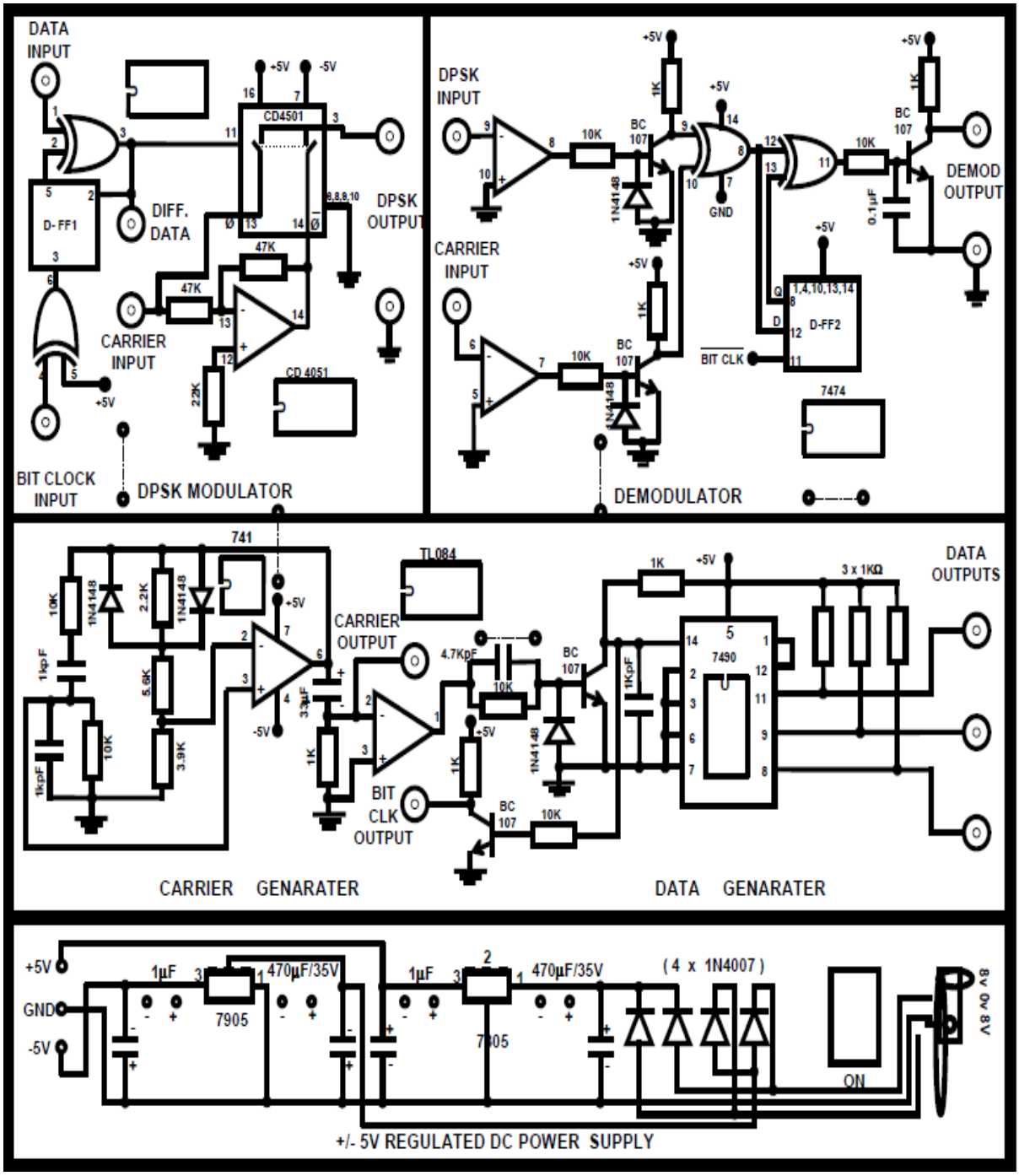
THEORY

The carrier wave signal is generated by a wein bridge oscillator around *** KHz at ±5V P-P sine wave using 741 the sine wave is convert into square wave using TL084 in comparator mode. The Transistor BC 107 converts the square signal to TTL levels. This is used as a basic bit clock or 180^0 for a mark and 0^0 for space. This Square wave is used as a clock input to a decade counter (IC 7490) which generates the modulating data outputs.

MODULATION

The Differential signal to the modulating signal is generated using an Exclusive -OR gate (7486) and a 1-bit delay circuit using D Flip Flop 7474 (It is shown in fig-1). CD 4051 is an analog multiplexer to which carrier is applied with and without 180° degrees Phase shift (created by using an operational amplifier connected in inverting amplifier mode) to the input of the TL084. Differential signal generated by Ex-OR gate (IC7486) is given to the multiplexer's control signal input. Depending upon the level of the control signal, carrier signal applied with or without phase shift is steered to the output. 1-bit delay generation of differential signal to the input is created by using a D-flip-flop(IC7474).

Circuit diagram:



DEMODULATION

During the demodulation, the data and carrier are recovered through a TL084 op amp in comparator mode . This level is brought to TTL level using a transistor and is applied to one input of an EX-OR gate. To the second input of the gate, carrier signal is applied after conversion into a +5V signal. So the EX-OR gate output is equivalent to the differential signal of the modulating data. This differential data is applied to one input of an Exclusive -OR gate and to the second input, after 1-bit delay the same signal is given. So the output of this Ex-OR gate is the recovered Modulating signal.

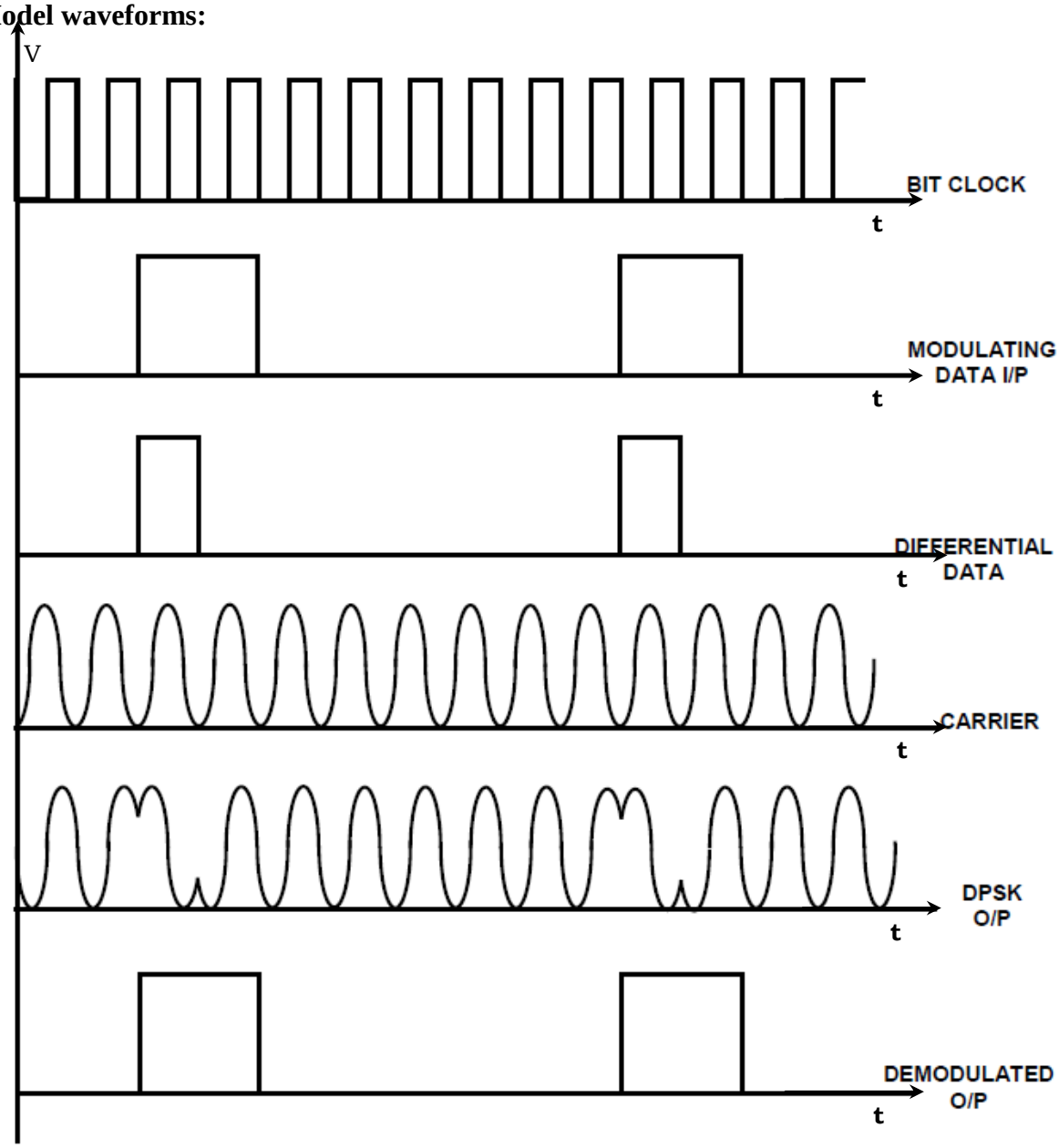
HARD WARE SPECIFICATIONS

1. Panel lay out diagram with components mounted on PCB /Panel
2. Built in variable DC power supplies +/ - 5V ,-350mA, the figures given.
3. ICs 741, 7490, 7474, CD4051, 7486 are provided on the trainer and the hardware details are given.
4. User Manual
5. Set of patch chords

6.EXPERIMENTAL PROCEDURE

1. 'Switch ON' the experimental board.
2. Check the carrier signal and the data generator signals initially.
3. Apply the carrier signal to the carrier input of the DPSK modulator and give the data generator to the data input of DPSK modulator and bit clock output to the input of DPSK modulator and Bit Clk O/P to Bit Clk input of modulator.
4. Observe the DPSK modulating output with respect to the input data generator signal of dual trace oscilloscope (observe the DPSK modulating signal on channel 1and the data generator signal on channel 2), and observe the DPSK Signal with respective to Differential data also.
5. Give the output of the DPSK modulator signal to the input of demodulator, give the bit clock output to the bit clock input to the demodulator and also give the carrier output to the carrier input of demodulator.
6. Observe the demodulator output with respect to data generator signal (modulating signal)

Model waveforms:



DPSK Signal Waveforms

PRECAUTIONS:

1. Avoid loose and wrong connections.
2. Readings should be noted without parallax error.

Result:

Thus the DPSK modulation and demodulation is performed and graphs were plotted.

VIVA QUESTIONS:

1. Define DPSK?
2. Mention the Advantages of DPSK?
3. Mention the Disadvantages of DPSK?
4. Draw the waveforms of DPSK?
5. Compare ASK, PSK, FSK& DPSK?
6. What are the Applications of DPSK?

6. FREQUENCY SHIFT KEYING

AIM

To study the generation of the Frequency Shift Keyed output and also to demodulate the FSK outpu with help of FUTURE TECH demonstration board.

INTRODUCTION

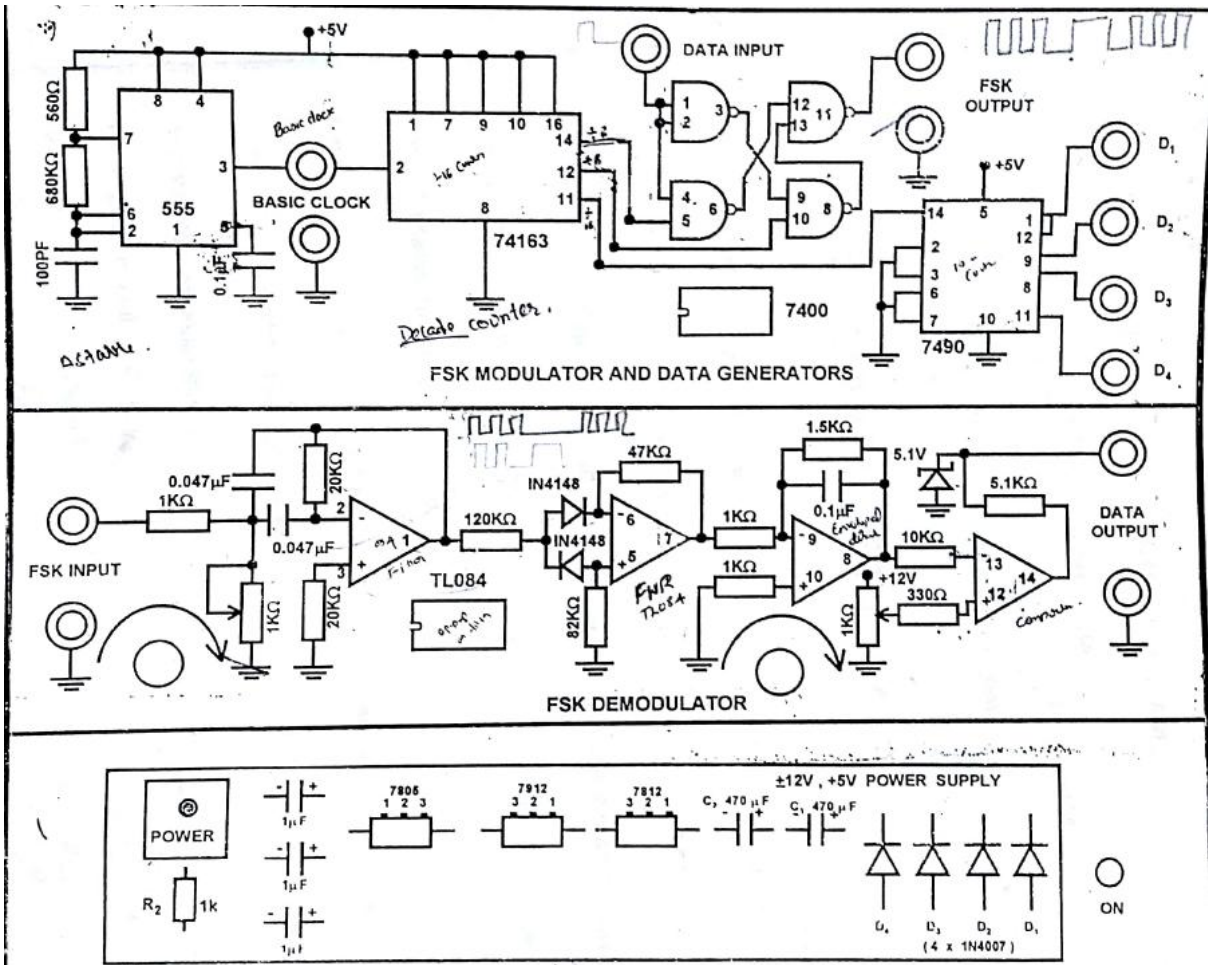
It would be quite possible to transmit teletype by the ordinary ON-OFF keying of the transmitter. In other words, we could use Amplitude modulation with pulses, ON corresponding to mark & OFF to space. Howeverm such a system has the inherent disadvantages that there is no real indication for the space. In addition, a system such as this would suffer from all the usual elements o Amplitude Modulation, as a result of which it is never used for automatic telegraphy (it is, of course, widely used for manual morse code CW operation). A system known as Frequency Shift Keying is generally used instead.

FSK is a system of frequency modulation, in it the nominal unmodulated carrier frequency corresponds to the mark condition, and a space is represented by a downward frequency shift. The amount was 850Hz in the original wideband FSK system designed for HF radio. For transmission by line or broad band systems, the current shift is 50Hz. This is known as narrow band FSK. or frequency modulated voice frequency telegraph (FM VFT). FSK is still often used for HF radio transmissions, with a frequency shift that is commonly 170Hz.

As with other forms of FM, the main advantage of the wide band system is greater noise immunity. while the narrow band systems are used to conserve the allocated frequency spectrum. Note that FSK may be thought of as an FM system in which the carrier frequency is midway between the mark and space frequencies, and modulation is by a square wave. In practice of course, only the fundamental frequency of the square wave is transmitted. and regeneration takes place in the receiver.

In the FSK generator, the frequency shift may be obtained by applying the varying DC output of the telegraph machine to a varactor diode in a crystal oscillator. At the receiving end, the signal s demultiplexed (if, as in common, FDM was used to send a number of telegraph or telex transmissions together) and applied to a standard phase discriminator.

Circuit Diagram:



From the discriminator, signals of either polarity will be available. After some pulse shaping, they are applied to the receiving teletype writer. If the telegraph transmission is by HF radio. The phase discriminator works at a (fairly low) intermediate frequency, although other methods are also possible for demodulation. An amplitude limiter is always used in the receiver, to take full advantage of the noise immunity of FSK.

THEORY

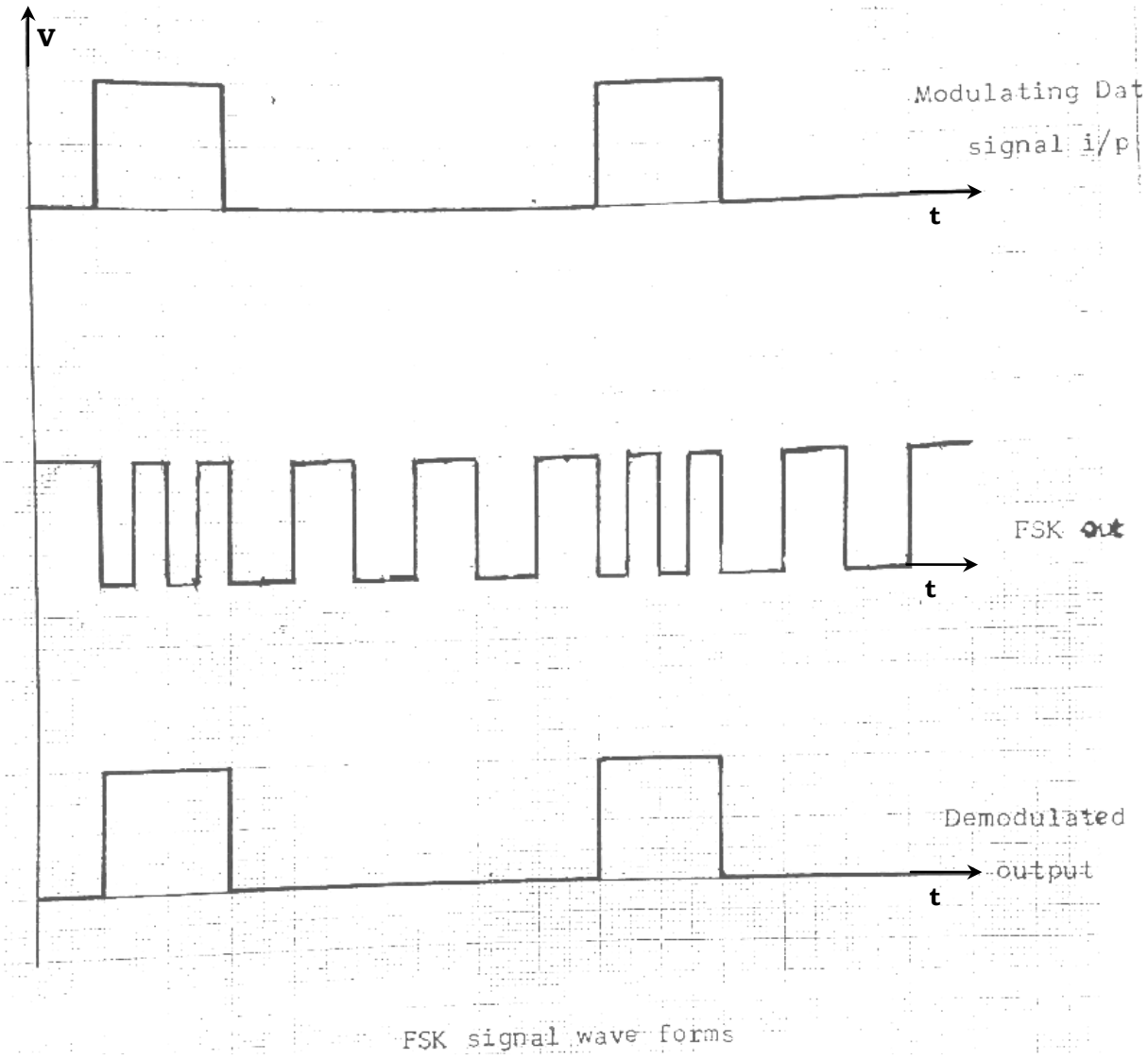
Panel diagram shows the FSK modulator and demodulator system. Basically a 555 IC is connected in Astable Multivibrator mode, generates a clock pulse of frequency determined by the values of RT and CT. This clock signal is given to a divided by 16 counter (74163 IC) which generates divided by 2,4,8 & 16 outputs of the input clock signal. In this system, divided by 2 & 8 outputs are taken as two carrier frequencies. So these are given to a FSK modulator constructed by using NAND gates. Divided by 16 output is given to a decade counter (IC 7490) which generates the modulating data signals. So depending on the level of the modulating data signal given to the FSK modulator, either divided by 2 or divided by 8 frequency outputs of the IC 74163 are transmitted to the output of the FSK modulator.

In the demodulator section, the FSK output is given to a high - Q tuned filter which is tuned to any frequency either divided by 2 or 8 of the outputs of 74163 counter. So the filter passes one frequency and stops the other frequency. This filter is constructed with operational amplifier TL084IC. The passed frequency is given to a full wave rectifier using operational amplifier TL084 IC, which rectifies and its output is given to an envelop detector which acts as a peak detector during pulse period. Then the output of the envelop detector is given to a comparator, its output is equivalent to the modulating data given at the input of the FSK modulator.

EXPERIMENTAL PROCEDURE

1. Connect the AC Adaptor to the mains and the other side to the Experimental Trainer.
2. Apply any one data output of the decade counter (7490IC) to the data input point of the FSK modulator and observe the same signal in one channel of a dual trace oscilloscope.
3. Observe the output of the FSK modulator on the second channel of the CRO.
4. During the demodulation, connect the FSK output to the input of the demodulator.
5. Adjust the potentiometers P1 & P2 until we get the demodulated output equivalent to the modulating data signal.

Model Waveforms:



FSK signal wave forms

PRECAUTIONS:

1. Avoid loose and wrong connections.
2. Readings should be noted without parallax error.

RESULT:

Thus the FSK modulation and demodulation is performed and graphs are plotted

VIVA QUESTIONS:

1. What is MSK?
2. For the given 8 bit data 10111010 draw the FSK output waveform.
3. Draw the constellation diagram of FSK.
4. What will happen if the same frequency is used for both the carriers?

7. QPSK MODULATION & DEMODULATION

AIM:

To generate a QPSK modulated signal for the given input data and its demodulated signal

INTRODUCTION & THEORY:

For Transmission of Digital signal over limited band width channel various methods of Modulation techniques were developed from simple FSK, PSK system to complex DPSK, DASK and QPSK system. In simple PSK system, the phase of the carrier was modulated such that the carrier phase was reversed during the logic zero bit (f_c =180^0) while the carrier without any phase shift (f_c=0) was transmitted during the logic "1" level or vice versa. This method is also known a BPSK or Bi phase shift keying. If f_d is the data rate, then the band width required for transmitting BPSK signal would be $2f_d$.

In QPSK, the phase of the carrier depends upon the pair of successive bits in the data stream. Thus, there are four possible combinations of bit pair viz 00, 01,10, and 11.
During each combination of bit pair the carrier frequency f_c is transmitted with quadrature phase difference as shown below in Table 1.

TABLE –1

Bit Pair	Phase of Carrier
00	fc ∠0^0
01	fc ∠90^0
10	fc ∠180^0
11	fc ∠270^0

Bit pair & corresponding carrier

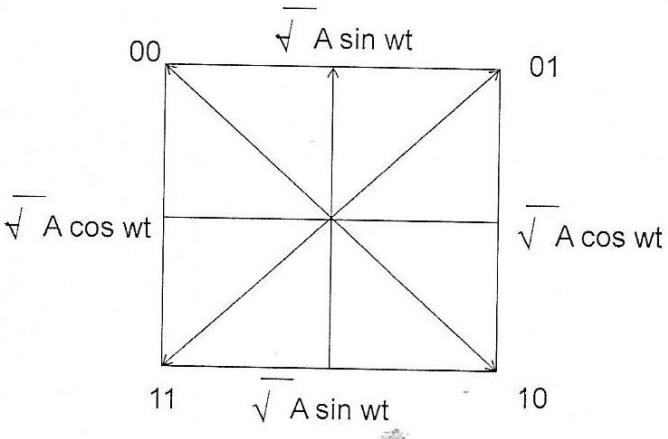


Fig 1: Phase diagram of carrier

The theoretical generation of QPSK is shown in the fig.1

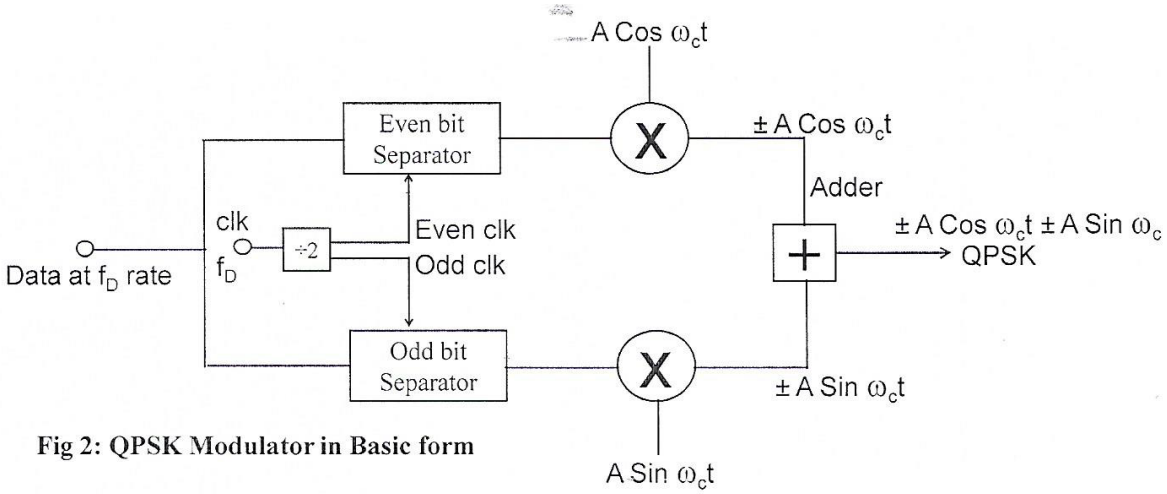


Fig 2: QPSK Modulator in Basic form

Principle of QPSK Generation:

The data coming at the rate of f_D the basic form of a QPSK Modulator is shown in Fig 2 is given to odd and even bit separators which are nothing but D Flip Flop driven by even clock and odd clock. The even clock and odd clock are generated by a toggle flip flop. The even and odd bit stream are generated at the rate of $f_D/2$.

This bit streams modulates the corresponding carrier A sin wt and A cos wt such that a phase shift of 180^0 is introduced for a logic '1' level as against logic 'O' level.

The adder gives the algebric sum of the modulated components. We observe from the Fig 1. phase diagram that, the resultant wave forms again will have 90^0 phase difference from successive bit pairs. It may also be noticed that succeeding bit pair will have only one bit change resulting only in $\pm 90^0$ phase shift of the resulting summer output.

In actual practice the quadriphase carriers can be generated and switched digitally depending upon the bit pair combination.

QPSK Receiver:

At the receiver end, the process of demodulation involves QPSK signal is modulated (using Balanced Modulation) again using recovered carrier signals (Cos ω_ct and Sin ω_ct). The resulting dual outputs are integrated to generate DC logic levels, of bit pairs. They are converted from parallel to serial signals by using time division switching.

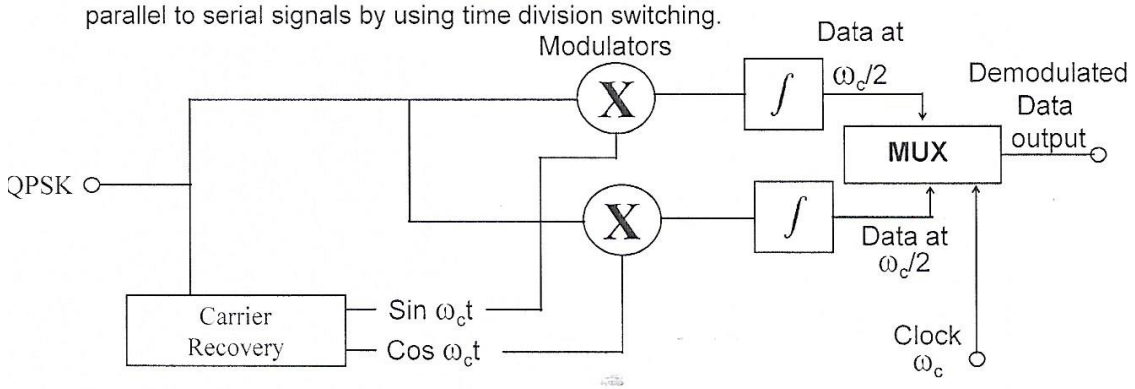
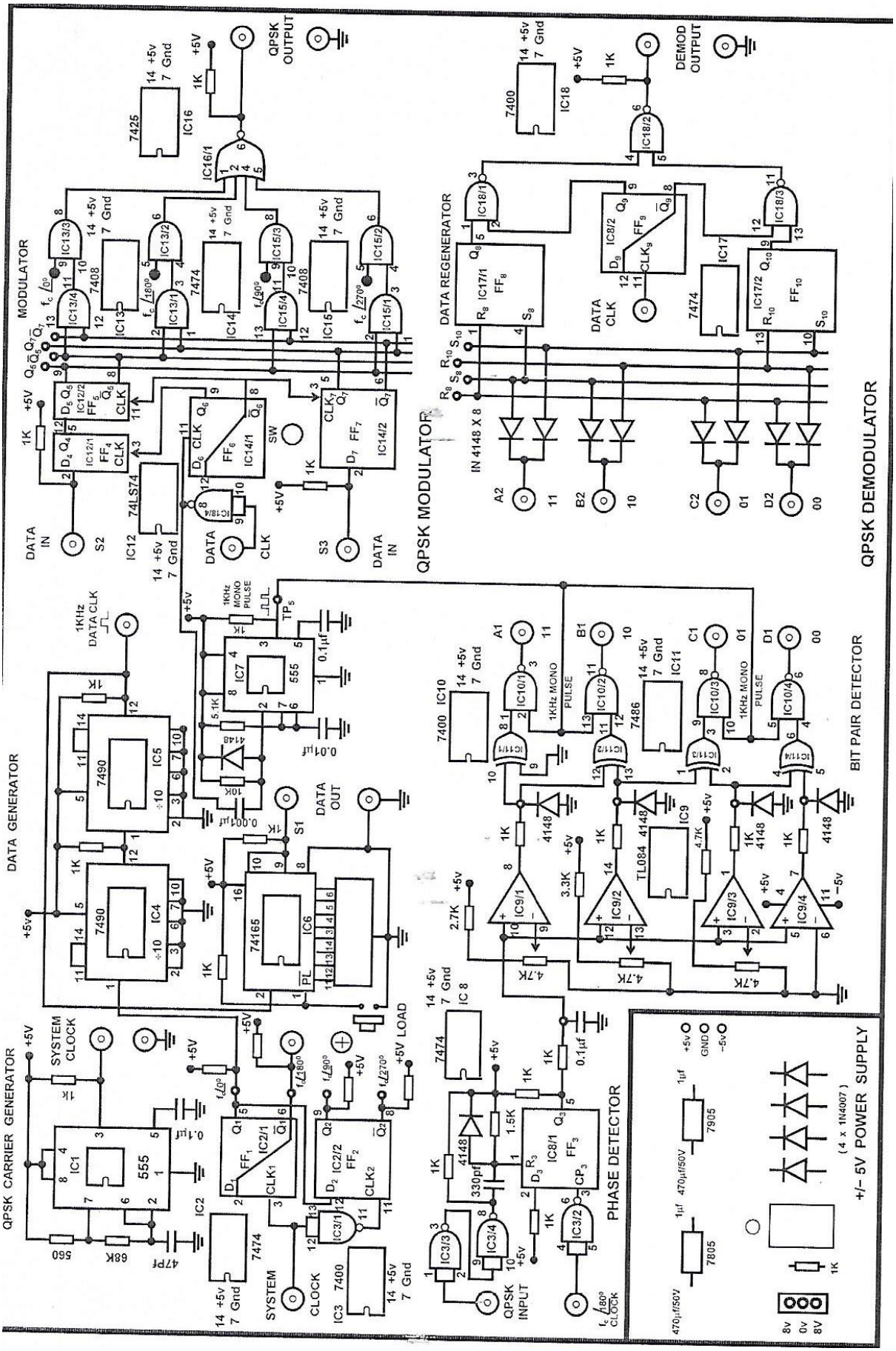


Fig3 : A QPSK receiver in basic form.



QPSK – Modulator:

Refer to the QPSK Modulator circuit diagram shown in Fig.4. The 555 timer circuit generates system clock a square wave frequency of approximately 200kHz. The quadri phase carriers $f_c \angle 0^0$, $f_c \angle 90^0$, $f_c \angle 180^0$ & $f_c \angle 270^0$ at approximately 100kHz are generates by two D – Flip Flops DFF1 & DFF2. These four carrier signals are given to four AND gates which are exclusively enabled by the presence of bit pair combination in the Data. The carrier switching with respect to the bit pair is shown in the table 2 below.

Table – 2

Bit pair b0b1	Carrier selected
00	fc $\angle 0^0$
01	fc $\angle 90^0$
10	fc $\angle 180^0$
11	fc $\angle 270^0$

The four AND gate outputs are 'OR' ed using a 4–input NOR gate followed by a NAND inverter. The resulting output is a QPSK modulated signal.

The data stream is generated at approx. 1kbps rate using a synchronous1kHz clock derived from 100kHz by two divide by 10 (IC 7490x2) circuit and a shift register (IC 74165) with parallel load and serial shift facility.

QPSK–DEMODULATOR:

The practical QPSK de modulator is shown in shown in fig:5.

In this method, a phase detector is employed to find the instantaneous phase of the QPSK signal with respect to a carrier clock $f_c \angle 180^0$. This consists of a D Flip Flop with $f_c \angle 180^0$ clock at the Clock Input and QPSK signal at the Reset input. Depending upon the negative going edge of the QPSK signal the D Flip Flop Resets Q to zero, while the positive edge at clk input R resets Q to 1 level as 'D' is pulled up to '1' level. Thus a series of pulses occur at the output of the D Flip Flop which are integrated using an RC Filter. The DC output available at the output of RC filter with respect to phase difference in the signals f_c 80^0 clk and QPSK signal is shown in Table 3.

Phase difference	Integrated DC output (Approx)	Corresponding transmitted bit fair combination
$\angle 0^0$	0.2V	00
$\angle 90^0$	1V	01
$\angle 180^0$	1.8V	10
$\angle 270^0$	3.0V	11

Table 3 : Output voltage Vs Phase of the carrier in QPSK with respect to the f_c 180^0 clock

The output of the phase detector and the corresponding Bit pair combination that generated the phase shift of the carrier is shown in Table 3. Therefore this bit pair combination is to be regenerated at the receiver before the serial data could be re constructed. For this purpose four comparators with different reference levels are provided. Their outputs are normalised to TTL levels using a resistance and clamping diode combination. Through a set of Four EX-NOR (EX-OR plus INV) gates pulses are generated in the respective phase periods of the carrier. The differentiated leading negative edges are used to appropriately 'Set' or 'Reset' two RS - Flip Flops (7474) which gives the bit pair information. This parallel Bit Pair information is transferred into serial bit pair (Referenced Data) using three NAND gates. The QPSK input is thus demodulated to reconstruct digital serial data.

Experimental Procedure:

1. Connect the QPSK Modulator -- Demodulator to Mains chord to AC source and switch on the trainer.
2. Check the phase difference of the Quadri Phase carries generated at the outputs of FFI and FF2.

Connect the output at TP1 to channel 1 of oscilloscope and synchronise the scope with channel1 and positive slope trigger.

Observe on channel 2 the phase shifted carriers at TP2, TP3 and TP4 w.r.t the carrier at TP1 and fill up the Table.

Signal at	Phase angle w.r.t Carrier at TP1
TP1	$\angle 0^0$
TP3	$\angle 90^0$
TP2	$\angle 180^0$
TP4	$\angle 270^0$

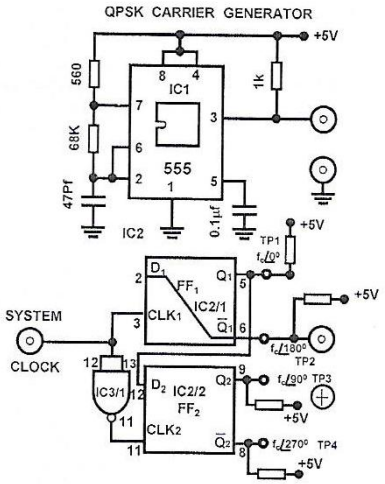


Table 4: Qudriphase carrier - phase angle differencier

2. Test the odd even bit separator for static bit levels.

The logic levels at socket S2 and S3 will determine the odd bit and even bit in the Data stream. Test the following Bit stream combinations as given in Table 5..

Note: S2 or S3 when open presents a Logic 1 level as the inputs are pulled up.

3. Test the selection of carriers w.r.t. the bit pair generation.
Observe on channel 1 carrier fc $\angle 180^0$ at TP1 connect on channel 2 the output of QPSK Modulator, observe the switched carrier as shown in Table 4.

TABLE 5

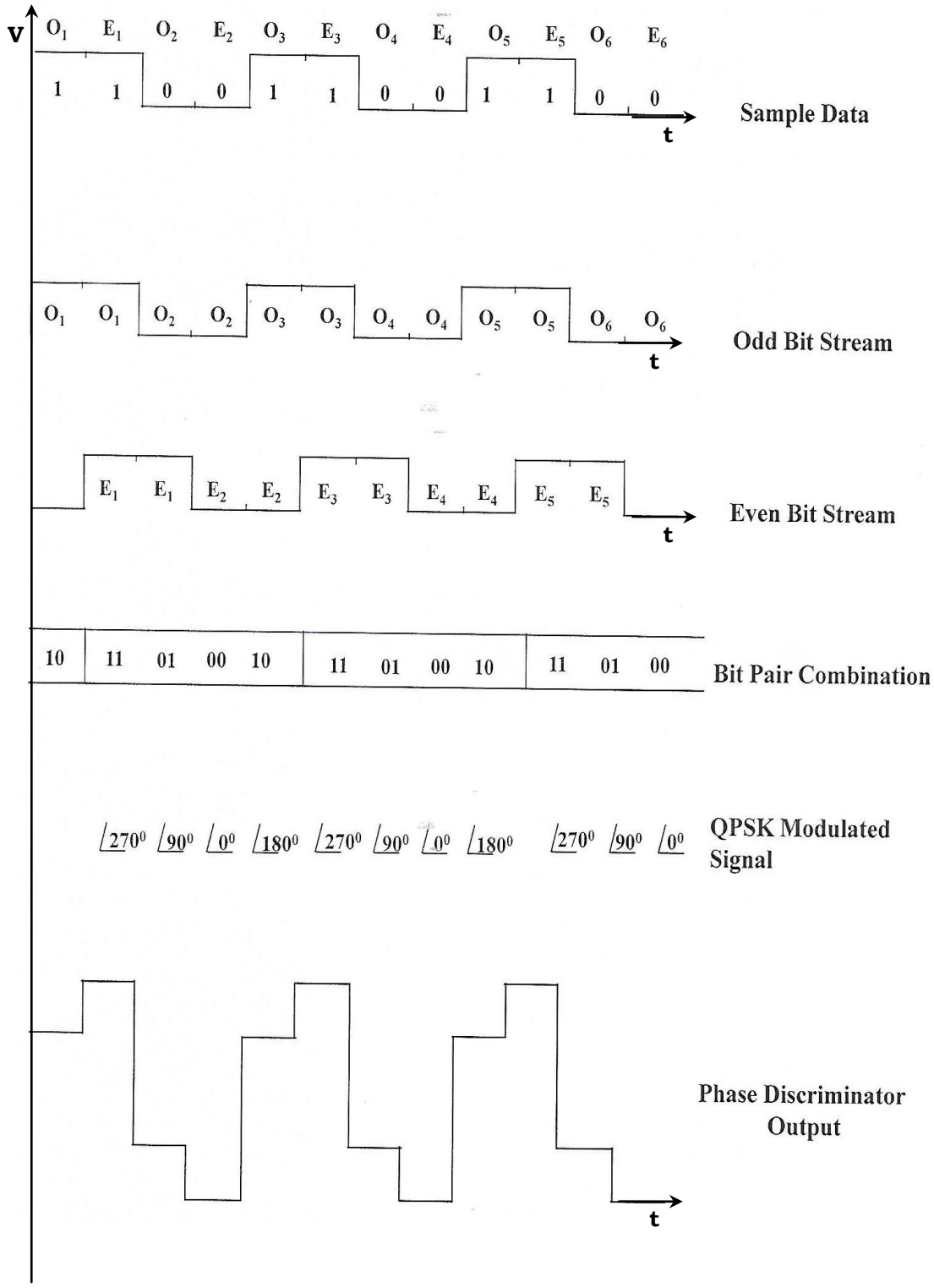
Socket S2	Socket S3	Phase angle of QPSK output w.r.t fc $\angle 180^0$ carrier on channel1
Gnd (0)	Gnd(0)	$f_c \angle 0^0$
Open (1)	Gnd (0)	$f_c \angle 180^0$
Gnd (0)	Open (1)	$f_c \angle 90^0$
Open (1)	Open (1)	$f_c \angle 270^0$

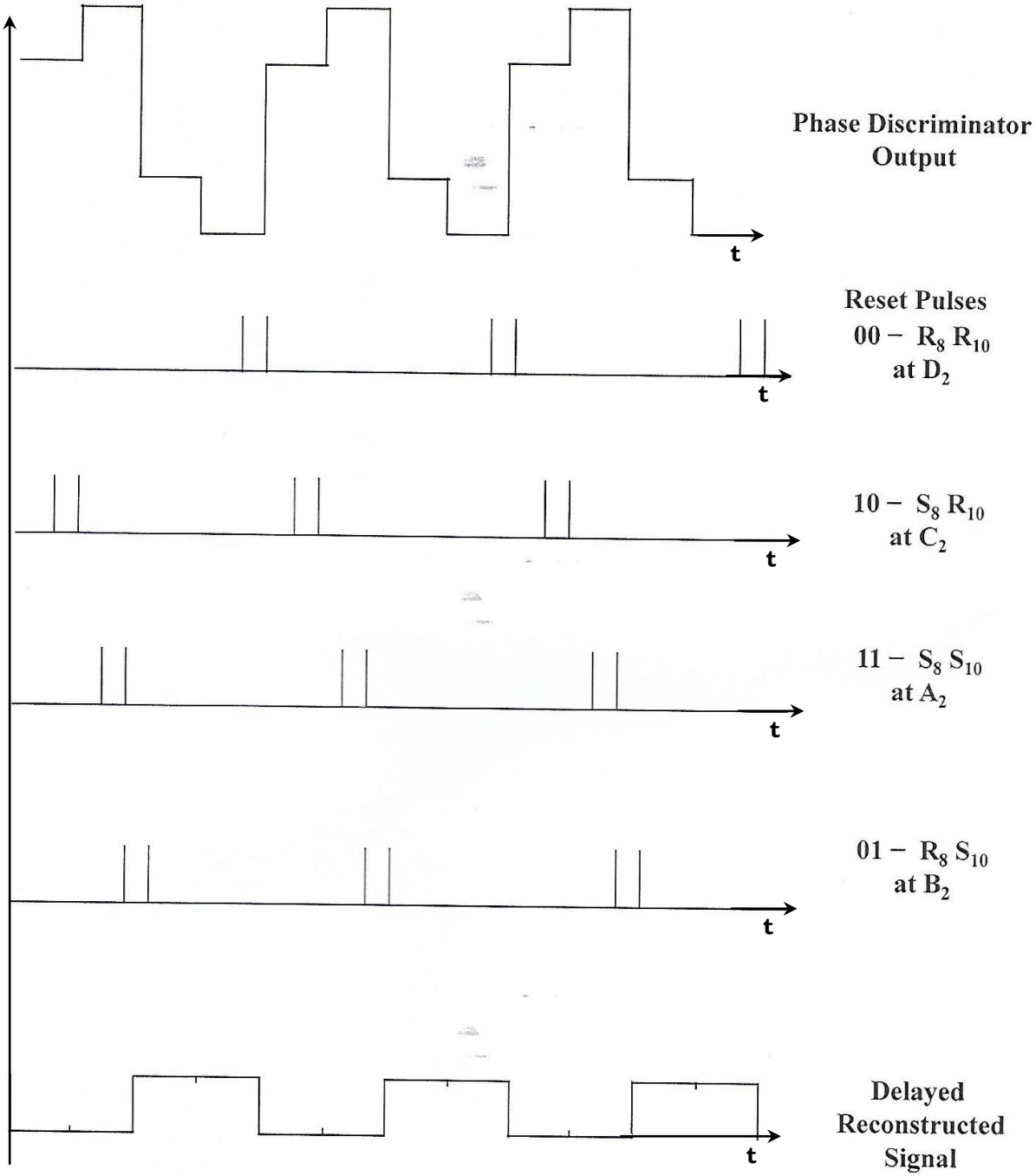
Table 6: Phase angle of carrier switched corresponding to the bit pair input

QPSK DEMODULATOR :

1. Connect QPSK output to the QPSK input and fc $\angle 180^0$ carrier at Clock input of Phase detector.
2. Observe phase detector output at Channel 1.
3. Connect bit pair detector output on Channel 2. We can observe small pulses corresponding to each bit pair combinations i.e., 11,10, 01 & 00 at A1, B1, C1 & D1 respectively. These pulses indicate no. of particular bit pair combinations for the selected 8–bit word.
4. Connect bit pair detector to data regenerator i.e A1 to A2; B1 to B2; C1 to C2 & D1 to D2. And data clock at clock input.
5. The output of data regenerator is the demodulated signal.

   (Note: This is the delayed output, because we have introduced one bit delay in the Modulator)


V
O1 E1 O2 E2 O3 E3 O4 E4 O5 E5 O6 E6
1 1 0 0 1 1 0 0 1 1 0 0
t
Sample Data
O1 O1 O2 O2 O3 O3 O4 O4 O5 O5 O6 O6
t
Odd Bit Stream
E1 E1 E2 E2 E3 E3 E4 E4 E5 E5
t
Even Bit Stream
10 11 01 00 10 11 01 00 10 11 01 00
Bit Pair Combination
270° 90° 0° 180° 270° 90° 0° 180° 270° 90° 0°
QPSK Modulated Signal
t
Phase Discriminator Output



Note : A Toggle Switch S is Provided to interchange Q6 and $\overline{Q6}$ so that proper initialization is done for modulation. If the output of the phase detector is improper change the switch position S to the other side.

Result :

Thus the QPSK modulated signal is generated and it is demodulated.

VIVA QUESTIONS:

1. Draw the constellation diagram of QPSK.
2. Give some applications of QPSK modulation scheme
3. Find the output of the following command. 5^ (2/3) – 25/ (2*3)
4. what is the relationship between 4 QAM and QPSK?
5. Design a simulink model for QPSK.

8. LINEAR BLOCK CODE - ENCODER & DECODER

AIM:
To Study the Hamming Code 7-bit Generation.

APPARATUS:

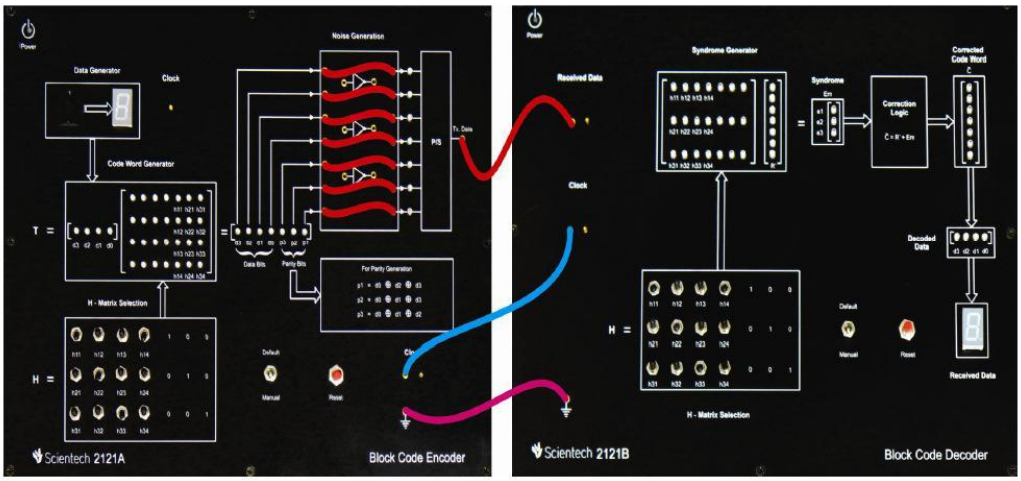
1. Linear Block Code- Encoder & Decoder Trainer Kit (Scientech 2121A & 2121B)
2. 2 mm Banana Cable
3. Regulated Power Supply

THEORY:

Error Detection and Correction:
Error detection is the ability to detect the presence of errors caused by noise or other impairments during transmission from the transmitter to the receiver. Error correction is the additional ability to reconstruct the original, error-free data. There are two basic ways to design the channel code and protocol for an error correcting system.

Linear block codes:
Linear block codes are conceptually simple codes that are basically an extension of single-bit parity check codes for error detection. A single-bit parity check code is one of the most common forms of detecting transmission errors. This code uses one extra bit in a block of n data bits to indicate whether the number of 1s in a block is odd or even. Thus, if a single error occurs, either the parity bit is corrupted or the number of detected 1s in the information bit sequence will be different from the number used to compute the parity bit: in either case the parity bit will not correspond to the number of detected 1s in the information bit sequence, so the single error is detected. Linear block codes extend this notion by using a larger number of parity bits to either detect more than one error or correct for one or more errors. Unfortunately linear block codes, along with convolutional codes, trade their error detection or correction capability for either andwidth expansion or a lower data rate, as will be discussed in more detail below. We will estrict our attention to binary codes, where both the original information and the corresponding code consist of bits taking a value of either 0 or 1.

BLOCK DIAGRAM:



PROCEDURE:

1. Connect the power supply mains cord to the Scientech 2121A and Scientech 2121B but do not turn ON the power supply until connections are made for this experiment.

2.Keep default/manual switch in Manual mode.

3.There are some conditions regarding H-Matrix selection manually which are:
Any row should not be identically selected like there should not all 1's or all 0's.

Each row selection should be different from other row.

The matrix should be so chosen that all the rows are distinct and consist of at least three 1's in them.

4.Switch 'On' the power supply and press reset button.

5.Check the clock pulse of 2 KHz on Oscilloscope at given test point.

6. At Scientech 2121A Block Code Encoder unit now select the data at seven Segment display with the help of BCD (binary coded decimal) switch.

7. Check the data at seven segment display and its binary equivalent (d3, d2, d1, d0), in the Code Word Generator block T where bit pattern is selected in the form of 8, 4, 2, 1 format.

8. Now set the H matrix are per the condition given in step 3. In Observation Table 3.1, some example sets are given (Set 1, Set2, Set3 and Set4). You can set your own matrix or you can choose any set from example sets and select the H Matrix as per the table.

6. After that check the H matrix in the form of H= [Ik] [P]; Identity matrix and Parity matrix corresponding to the selected set as given in the Observation Table 3.1.

7. Check the massage signal in the form of (d3, d2, d1, d0, p3, p2, p1) and verify the status of 'Parity Bits' (p3, p2, p1) as per the equations given for parity generation (see bservation Table 3.1).

8. Connect 2mm patch cords between horizontal bit stream and p/s block as per the connections diagram.

9. Observe the bit pattern output of codeword Generator at vertical 7-bit stream.

10. Now connect the Data output to the Data In of 2121B which is block code decoder.

11. Now connect the clock and ground of 2121A to 2121B via a 2mm patch cord.

12. Now set the H-Matrix section of 2121B Block code Decoder unit as per the same set what you have chose for 2121A Encoder unit. Refer the Observation Table 3.1.

13. Now first set Data '0' at Encoder unit and press reset switch until you get same decoded data on LED display and as well as at the seven segment display in numeric form. Once you get the same data 0 at decoder unit you can vary BCD switch to get the sequential data from 0-9.

14. For any selected data from 0-9, check the H matrix in the form of H= [P] [Ik]; Parity matrix and Identity matrix as given in the Observation Table 3.1

15. Also check the massage signal in vertical matrix 'R' in the form of (d3, d2, d1, d0, p3, p2, p1) and check the status of Syndrome Em. As there is no error in the bits it will show (0 0 0).

16. Check the corrected code word and match it with the code word of Encoder unit.

17. Also check the Decode Bits (d3, d2, d1, d0) and match with the data at Encoder unit.

Equations for Parity Generation:

$p1 = d0 \oplus d2 \oplus d3$

$p2 = d0 \oplus d2 \oplus d3$

$p2 = d0 \oplus d1 \oplus d2$

Code Word Generator:

Identity Matrix				Parity Matrix		

Observation Table:

Decimal	Binary
7 Segment	d3 d2 d1 d0
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	

Code Word
d3 d2 d1 d0 p3 p2 p1

RESULT:

Linear Block Code encoding and decoding are verified.

VIVA QUESTIONS:

1 WHAT ARE THE BLOCK CODES EXPLAIN THE MECHANISM OF ENCODING AND DECODING IN LINEAR BLOCK?

2 WHAT ARE THE PROPERTIES OF LINEAR BLOCK CODE?

3 WHAT IS MEANT BY LINEAR BLOCK CODES?

4 HOW IS LINEAR BLOCK CODE CALCULATED?

9. CONVOLUTION CODE- ENCODER AND DECODER

Aim:

To study the Convolution Encoding and Code tree of Encoder for K=3 With Rate = ½ & Study of Decoder with State and Trellis Diagram for K = 3 With Rate = ½

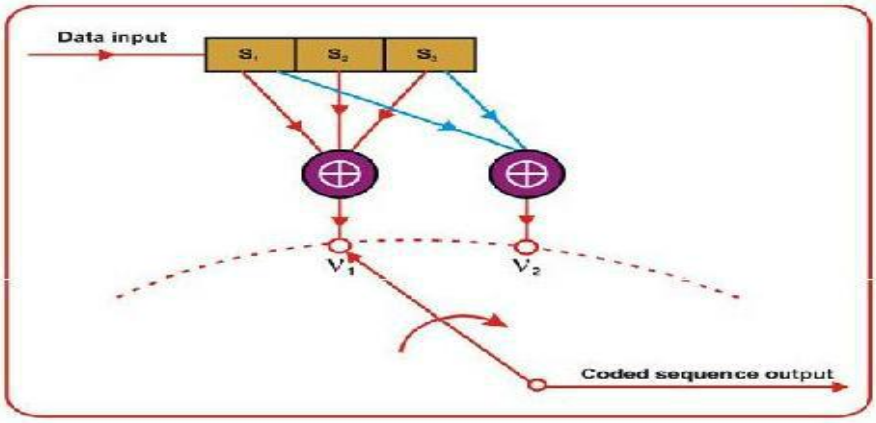
.

Apparatus Required:

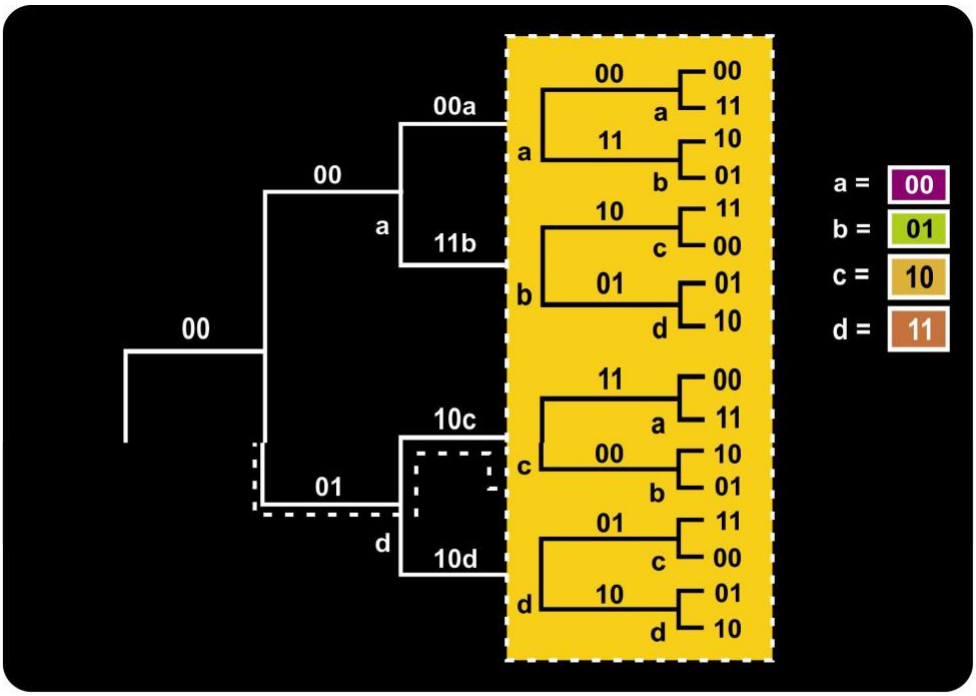
1. ST2122A & ST2122B Convolution Encoding and Decoding Kit
2. 2 mm Banana cable

Theory:

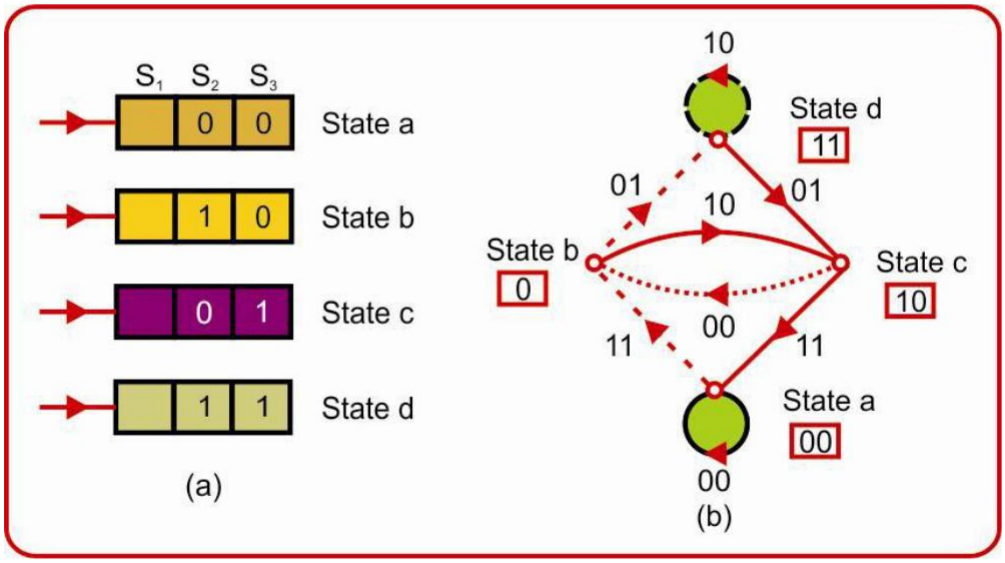
Coding Techniques are used for several reasons: Reduction of dc wandering, Suppression of inter-symbol interference, and reduce error rate. Noise within a transmission channel inevitably causes discrepancies or error between the channel input and channel output. Convolution codes were first introduced by Elias in 1955 as an alternative to block codes. These problems are of engineering interest in the transmission of digital data the coding schemes are used for error detection and correction. In the block coding techniques, the encoder splits up incoming data stream into blocks of finite-number digits and processes each block by adding extra bits (called redundancy) according to a pre defined algorithm. The output of the encoder is a codeword with another finite number of digits. In the convolution coding techniques, the encoder processes the incoming data stream continuously while its decoder employs the Viterbi algorithm among others



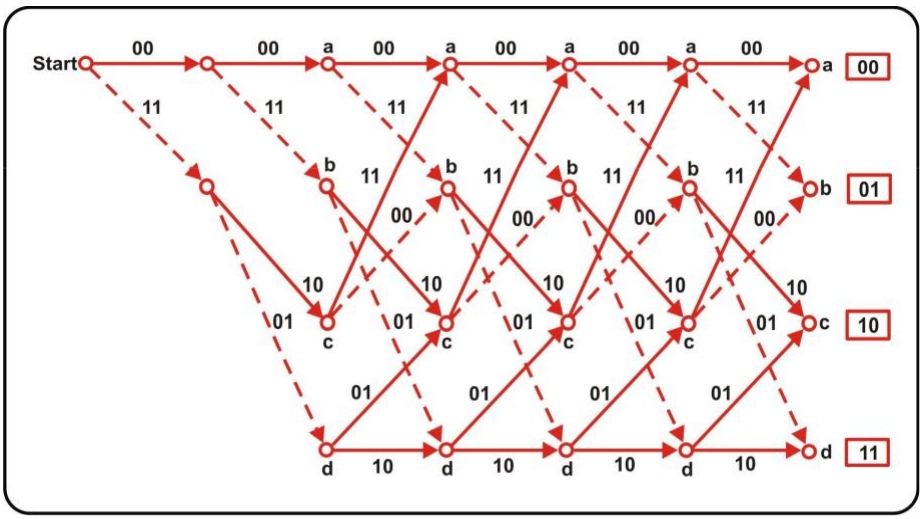
Convolution Coder



Code Tree for Coder

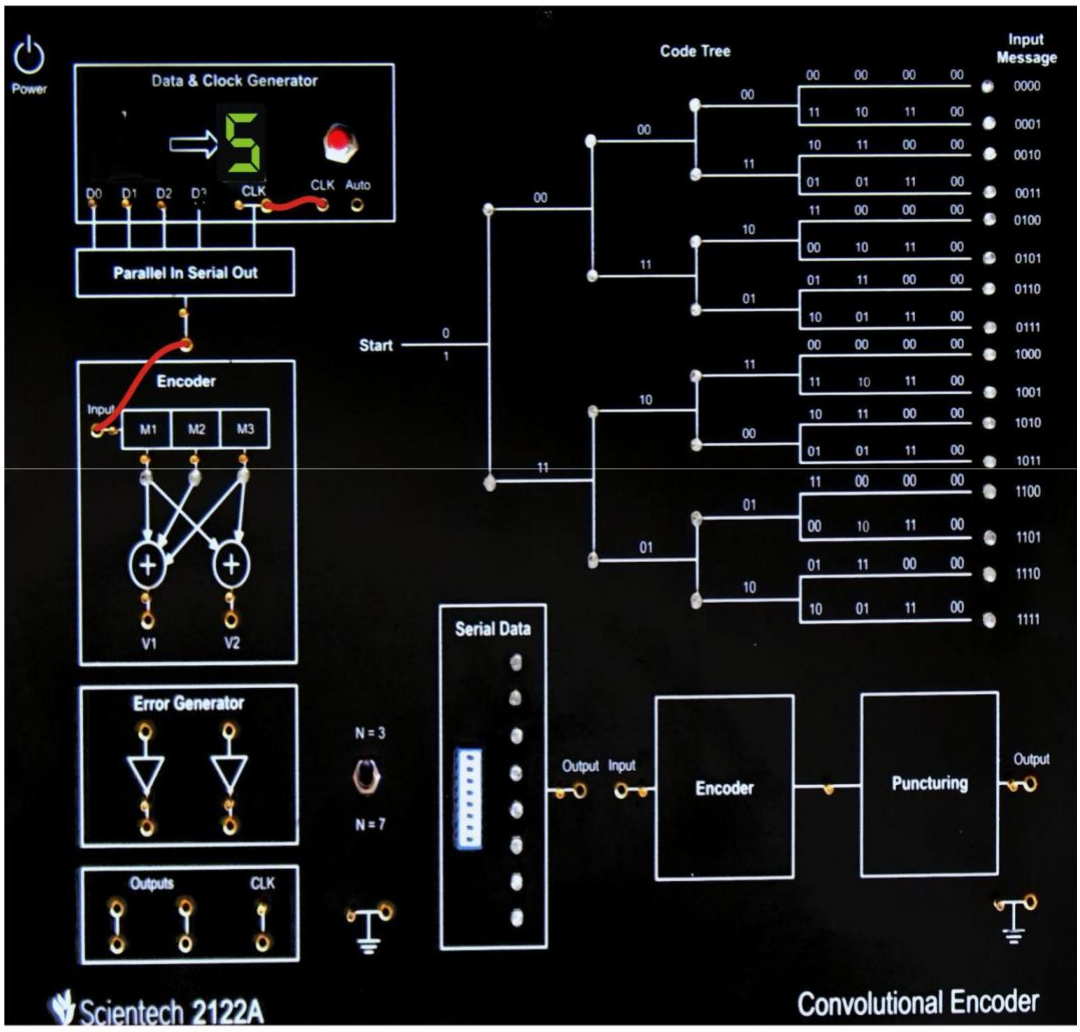


State Diagram for Coder



Trellis diagram for the coder

Connection diagram:



Connection diagram for convolution encoder

Procedure for Encoder:

1. Connect all the patch cord as per above image.
2. Connect the power supply mains cord to the Scientech 2122A, but do not turn ON the power supply until connections are made for this experiment.
3. Keep switch at "N = 3" mode in Scientech 2122A.
4. Switch 'On' the power supply (Using Touch Switch) of Scientech 2122A and press reset button.
5. Initially all the LEDs of Scientech 2122A should be off.
6. Now, select the data at seven segment display with the help of BCD (binary coded decimal) switch. (Note: To select data from 9 to 15 then remove "D3" and refer table 1.0).
7. Check the data at seven segment display and its binary equivalent (d3, d2, d1, d0), in the "Data and Clock Generator block" where bit pattern is selected in the form of 8, 4, 2, 1 format and output is shown in Table 1.1.

Data Table1.1

Data	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

8. For experiment we have select data at seven segments display is "5". So for this data the corresponding two outputs (V1 and V2) and memory state (M1, M2 and M3) are shown in Table1.2

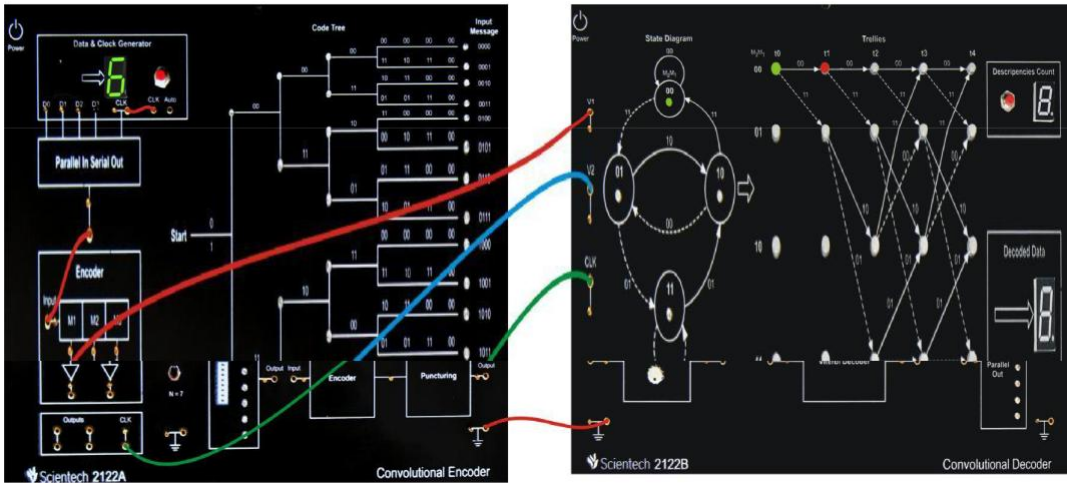
Equations for output: Table for Data = "5" (0101)

Output Table1.2

Clock	Memory M1	Memory M2	Memory M3	Output V1	Output V2
Initial	0	0	0	0	0
1	0	0	0	0	0
2	1	0	0	1	1
3	0	1	0	1	0
4	1	0	1	0	0
5	0	1	0	1	0
6	0	0	1	1	1
7	0	0	0	0	0

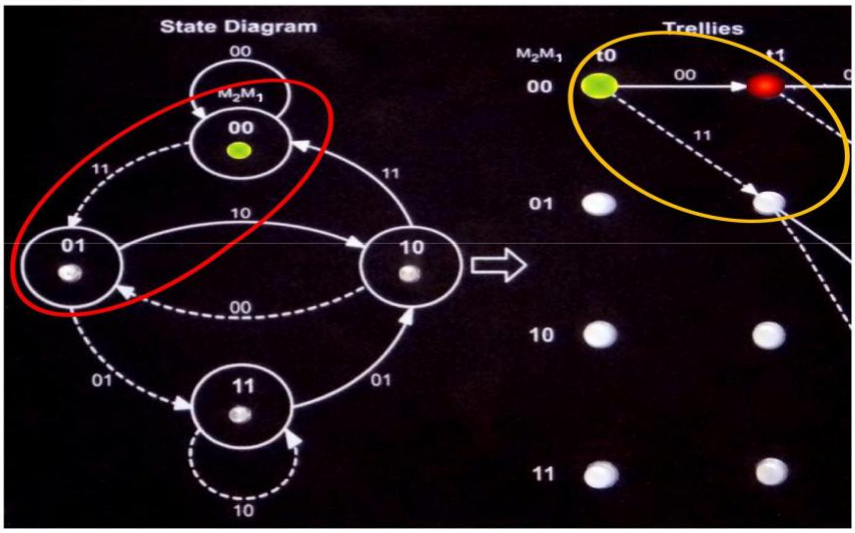
9. Now ,Press clock switch for nest and check the above output on Scientech 2122 A Encoder and code tree Section.
10. Repeat Step 9 up to 7 clocks
11. Also, if user wants to check data in auto clock mode then connect patch card one to auto mode.
12. For code Data = 5 the LED Statues on code tree.

Connection Diagram for Convolution Decoder:



Procedure for Decoder:

1. Connect all the patch cord as per above image.
2. Connect the power supply mains cord to the Scientech 2122A, but do not turn ON the power Supply until connections are made for this experiment.
3. Keep Switch at " N=3" mode in both trainer.
4. Switch 'ON' the power supply (Using touch Switch) of Scientech 2122A and press reset button.
5. Initially all the LEDs of Scientech 2122A should be off
6. Now, select the data at seven segment display with the help of BCD (binary coded Decimal) Switch. (Note: To select data from 9 to 15 then remove "D3" and refer table1.0)
7. Check the data at seven display and its binary equivalent (d3,d2,d1,d0), in the Data clock generator block. Where bit pattern is selected in the form of 8,4,2,1 format and output is shown in table1.0
8. Switch ON the power supply of Scientech 2122B and press reset button.
9. Initially if there is no error, LED "00" and "01" will blink in state diagram and LED to ("00") on is green colour and its corresponding two LED will blink in RED Color .

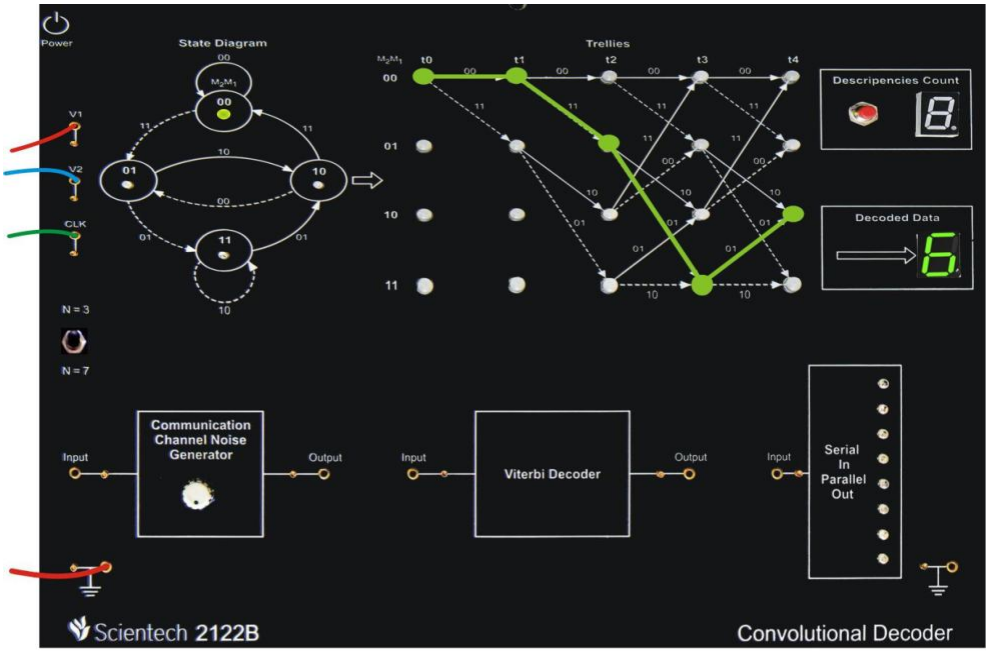


10. Now , as we have selected the data at seven segment display is "6" . So for this data output table will be as shown below.
    Table for data =6 (0110)

Output Table1.3

Clock	Memory M1	Memory M2	Memory M3	Output V1	Output V2
Initial	0	0	0	0	0
1	0	0	0	0	0
2	1	0	0	1	1
3	1	1	0	0	1
4	0	1	1	0	1
5	0	0	1	1	1
6	0	0	0	0	0
7	0	0	0	0	0

11. Now, press clock switch for next clock and check the above output on scientech 2122A encoder and code tree section and scientech 2122B state diagram and Trellis Section.
12. In Scientech 2122B the state diagram and trellis will indicate current state and next two possible states.
13. Up to four clock LED status will be shown below and after next three clock data will be Display on decoded data seven segment.



Decoded Data

Results:

The study of convolution encoding and decoding is verified.

VIVA QUESTIONS:

1 Which of them is not a convolution decoding method ?

2 Which of the following are method used for representing convolution encoder ?

3 Where are convolution codes used ?

4 Which decoding method involves ?

SOFTWARE EXPERIMENTS:

1. AMPLITUDE SHIFT KEYING

AIM:-

To plot the wave form for Binary Amplitude Shift Keying (BASK) signal using MATLAB for a stream of bits.

THEORY:-

Amplitude Shift Keying (ASK) is the digital modulation technique. In amplitude shift keying, the amplitude of the carrier signal is varied to create signal elements. Both frequency and phase remain constant while the amplitude changes. In ASK, the amplitude of the carrier assumes one of the two amplitudes dependent on the logic states of the input bit stream. This modulated signal can be expressed as:

$$x_c(t) = \begin{cases} 0 & \text{symbol "0"} \\ A\cos\omega_c t & \text{symbol "1"} \end{cases}$$

Amplitude shift keying (ASK) in the context of digital signal communications is a modulation process, which imparts to a sinusoid two or more discrete amplitude levels. These are related to the number of levels adopted by the digital message. For a binary message sequence there are two levels, one of which is typically zero. Thus the modulated waveform consists of bursts of a sinusoid. Figure 1 illustrates a binary ASK signal (lower), together with the binary sequence which initiated it (upper). Neither signal has been band limited.

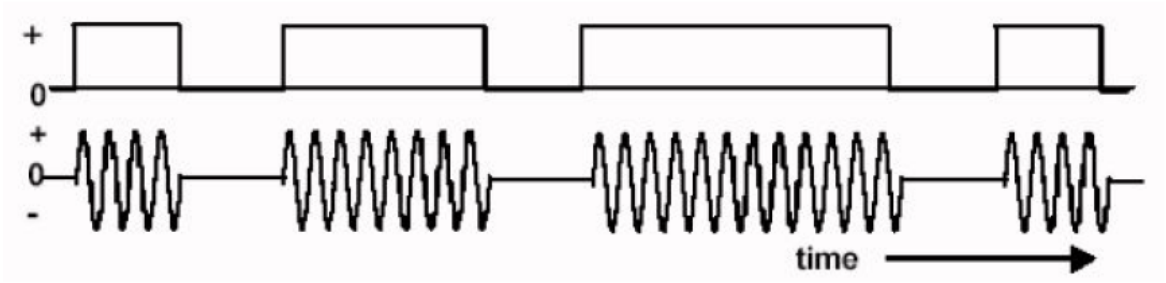


Fig: an ASK signal (below) and the message (above)

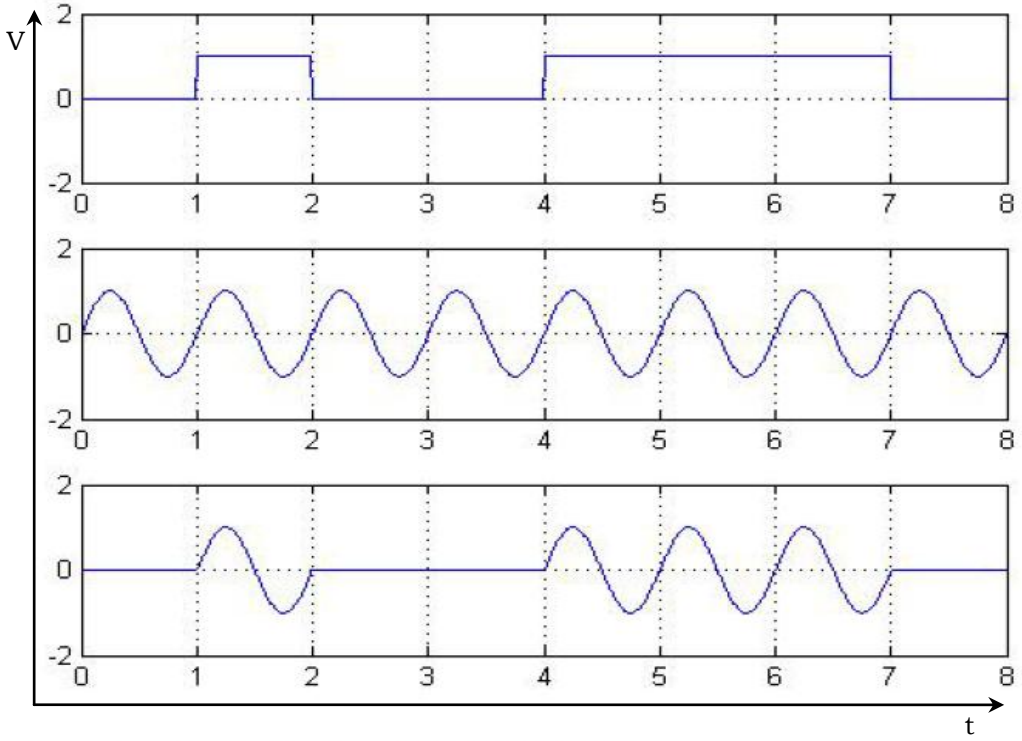
There are sharp discontinuities shown at the transition points. These result in the signal having an unnecessarily wide bandwidth. Band limiting is generally introduced before transmission, in which case these discontinuities would be 'rounded off'. The band limiting may be applied to the digital message, or the modulated signal itself. The data rate is often made a sub-multiple of the carrier frequency. This has been done in the waveform of Fig.

MATLAB PROGRAM:-

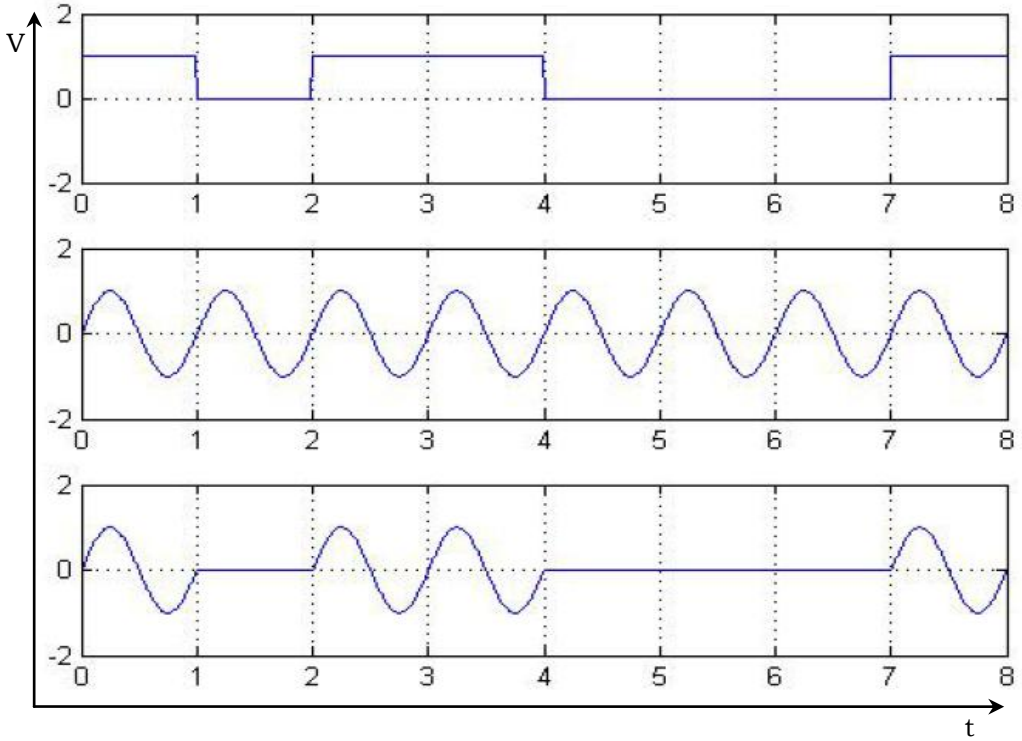
```
clear;
clc;
b = input('Enter the Bit stream \n ');   %b = [0 1 0 1 1 1 0];
n = length(b);
t = 0:.01:n;
x = 1:1:(n+1)*100;
for i = 1:n
   for j = i:.1:i+1
      bw(x(i*100:(i+1)*100)) = b(i);
   end
end
bw = bw(100:end);
sint = sin(2*pi*t);
st = bw.*sint;
subplot(3,1,1)
plot(t,bw)
grid on ; axis([0 n -2 +2])
subplot(3,1,2)
plot(t,sint)
grid on ; axis([0 n -2 +2])
subplot(3,1,3)
plot(t,st)
grid on ; axis([0 n -2 +2])
```

OBSERVATION:-

Output waveform for the bit stream [0 1 0 0 1 1 1 0]



Output waveform for the bit stream [1 0 1 1 0 0 0 1]



Result:

The program for ASK modulation and demodulation has been simulated in MATLAB and necessary graphs are plotted

VIVA QUESTIONS:

1. Compare ASK and PSK.

2. List the advantages of ASK.

3. Applications of ASK.

2. PHASE SHIFT KEYING

AIM:-

To plot the wave form for Binary Phase Shift Keying signal (BPSK) using MATLAB for a stream of bits.

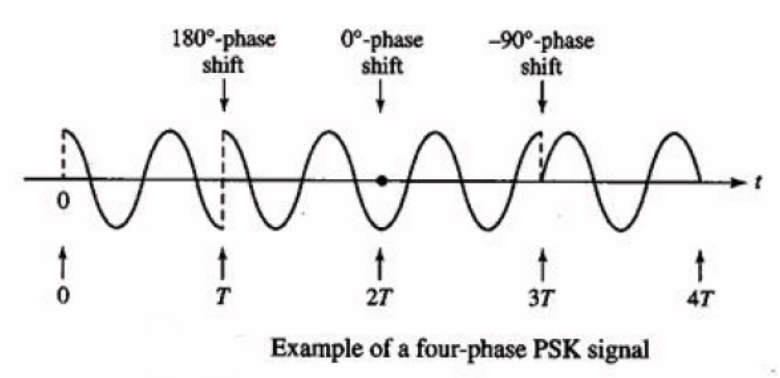
THEORY:-

In carrier-phase modulation, the information that is transmitted over a communication channel is impressed on the phase of the carrier. Science the range of the carrier phase is $0 \leq \theta \leq 2\Pi$,the carrier phases used to transmit digital information via digital-phase modulation are $\theta_m=2\Pi m/M$, for m=0,1,2…..,M-1.Thus for binary phase modulation(M=2),the two carrier phase are $\theta_0 =0$ and $\theta_1 = \Pi$ radian. For M-array phase modulation=$2^{k,}$ where k is the number of information bits per transmitted symbol.

The general representation of a set of M carrier-phase-modulated signal waveforms is

$u_m(t) = AgT(t) \cos(2\Pi fct+2\Pi m/M)$, m=0,1,…….,M-1

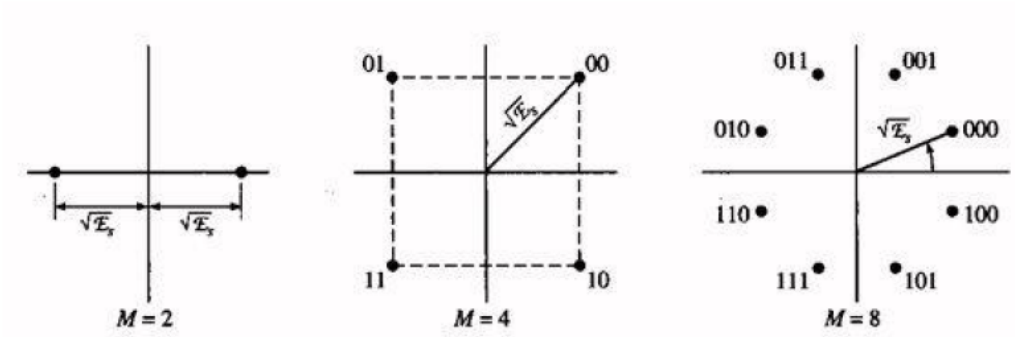
Where, gT(t) is the transmitting filter pulse shape, which determines the spectral characteristics of the transmitted signal, and A is the signal amplitude. This type of digital phase modulation is called phase-shift-keying.



Example of a four-phase PSK signal

Signal point constellations for M=2, 4 and 8 are illustrated in figure. We observe that binary phase modulation is identical to binary PAM (binary antipodal signals).The mapping or assignment, of k information bits into the M= 2^k possible phases may be done in a number of ways. The preferred assignment is to Gray in coding, in which adjacent phases differ by one binary digit, as illustrated

below in the figure. Consequently, only a single bit error occurs in the k-bit sequence with Gray encoding when noise causes the incorrect selection of an adjacent phase to the transmitted phase



PSK signal constellations

In figure shows that, block diagram of M=4 PSK system. The uniform random number generator fed to the 4-PSK mapper and also fed to the compare. The 4-PSK mapper split up into two phases. On the other hand, Gaussian RNG adds to the modulator. The two phases are fed to the detector. The output goes to the compare. The Uniform random number generator and detector also fed to the detector and finally fed to the bit-error counter and symbol-error counter.

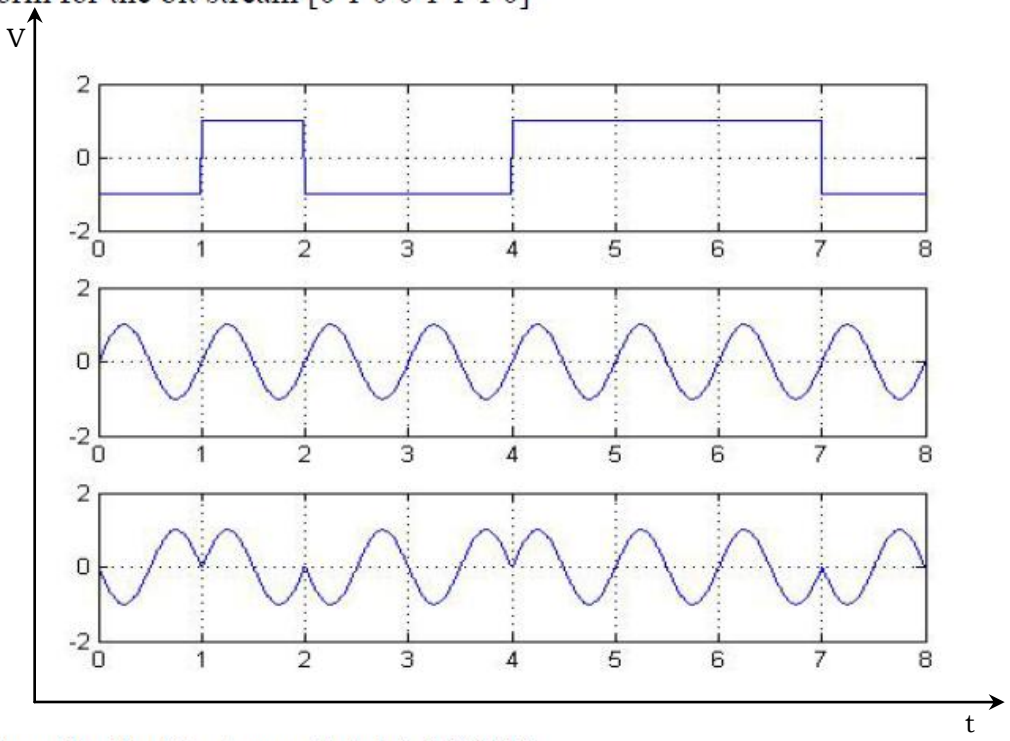
MATLAB PROGRAM:-

```
clear;
clc;
b = input('Enter the Bit stream \n ');          %b = [0 1 0 1 1 1 0];
n = length(b);
t = 0:.01:n;
x = 1:1:(n+1)*100;
for i = 1:n
   if (b(i) == 0)
      b_p(i) = -1;
   else
      b_p(i) = 1;
   end
   for j = i:.1:i+1
      bw(x(i*100:(i+1)*100)) = b_p(i);
   end
end
```

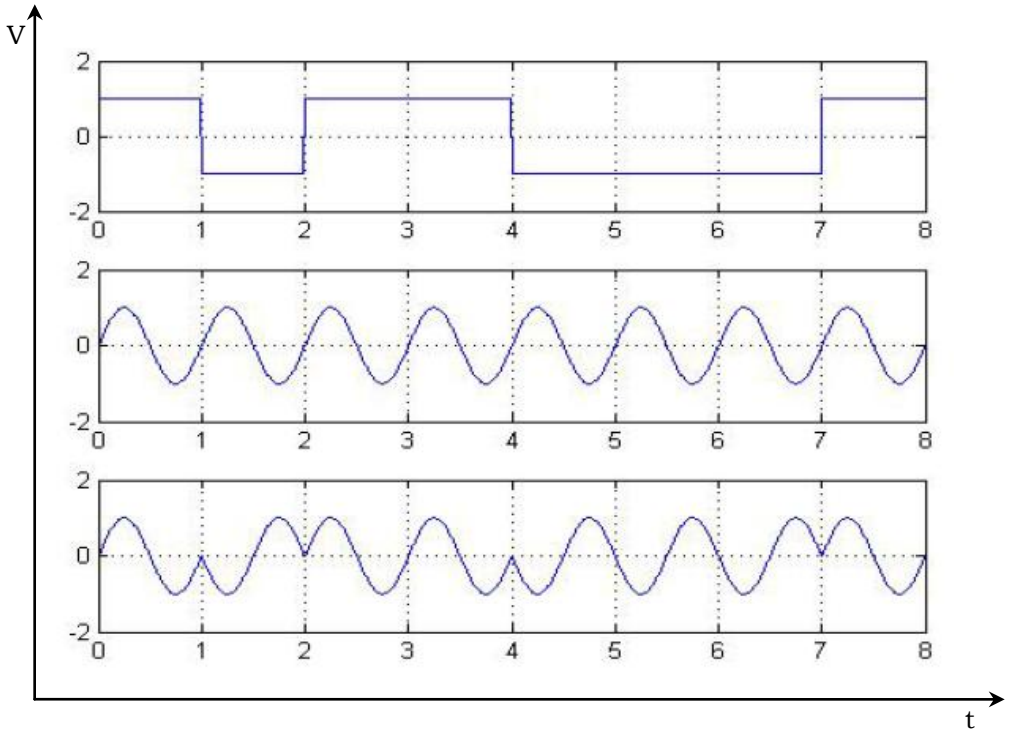
```
bw = bw(100:end);
sint = sin(2*pi*t);
st = bw.*sint;
subplot(3,1,1)
plot(t,bw)
grid on ; axis([0 n -2 +2])
subplot(3,1,2)
plot(t,sint)
grid on ; axis([0 n -2 +2])
subplot(3,1,3)
plot(t,st)
grid on ; axis([0 n -2 +2])
```

OBSERVATION:-

Output waveform for the bit stream [0 1 0 0 1 1 1 0]



Output waveform for the bit stream [1 0 1 1 0 0 0 1]



Result

The program for PSK modulation and demodulation has been simulated in MATLAB and necessary graphs are plotted.

VIVA QUESTIONS:

1. Compare FSK and PSK.

2. List the Characteristics of TL084 op-amp.

3. Compare TL084 op amp with IC 741 op amp.

4. What do we infer from constellation diagrams of various modulation schemes?

3. TIME DIVISION MULTIPLEXING

Aim

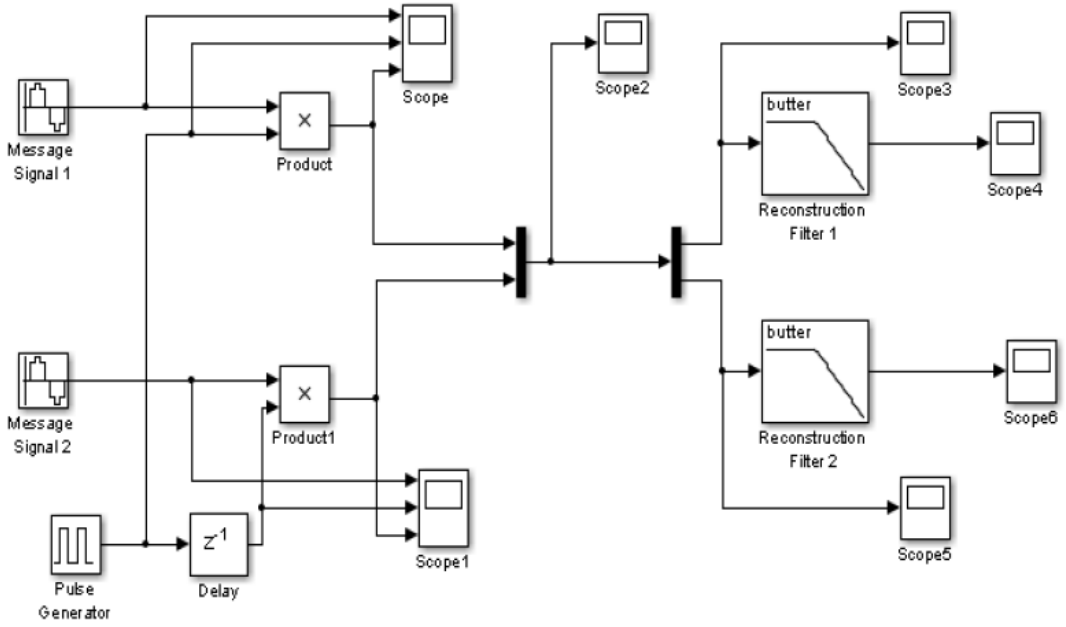
To perform the Time Division Multiplexing using Matlab Simulink.

Apparatus Required

a) Hardware Tools: Computer system

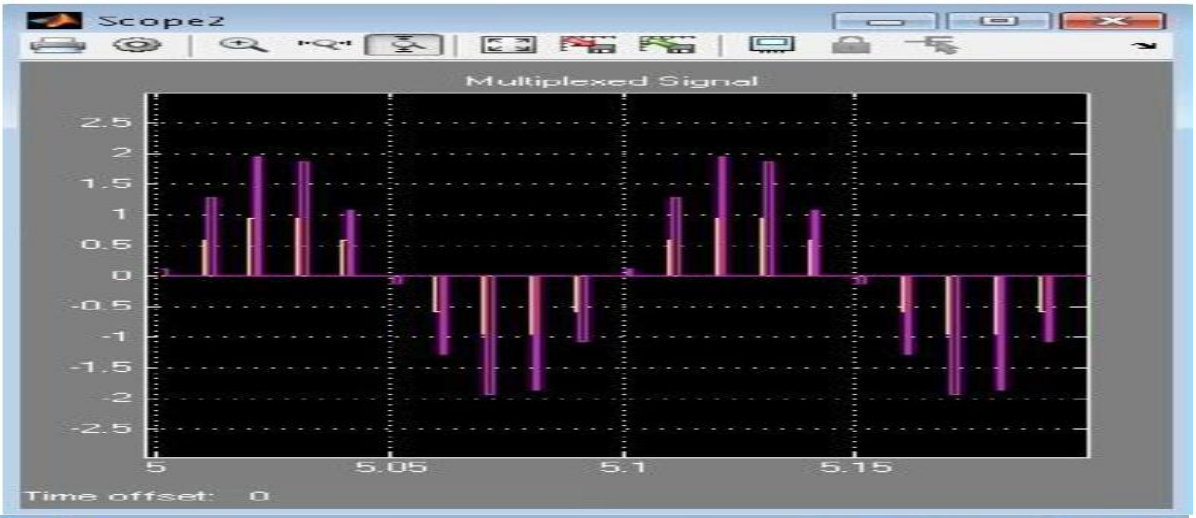
b) Software Tool: MATLAB 7.0 or Upgraded Version

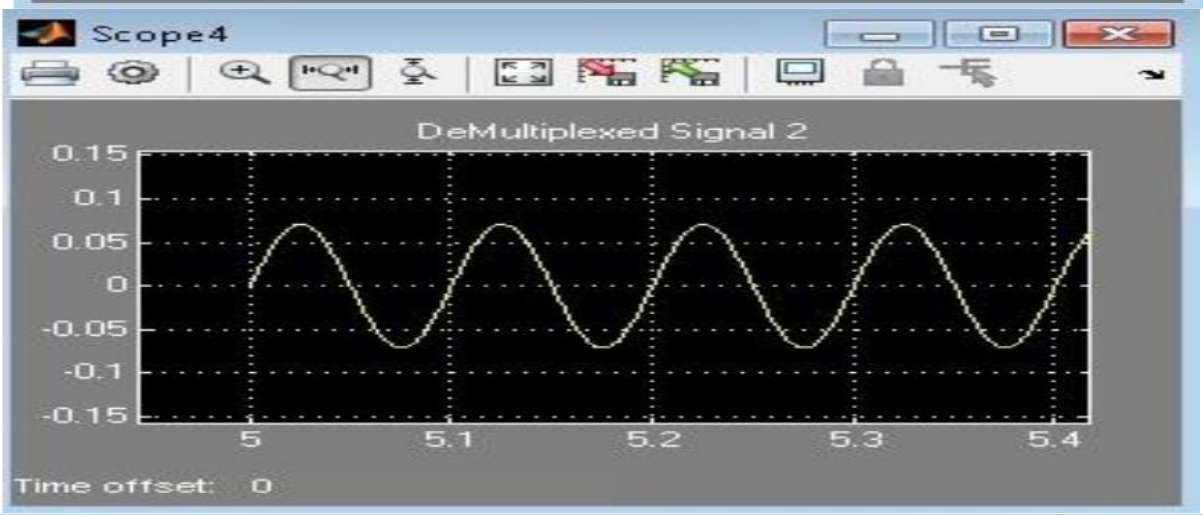
Simulink Model

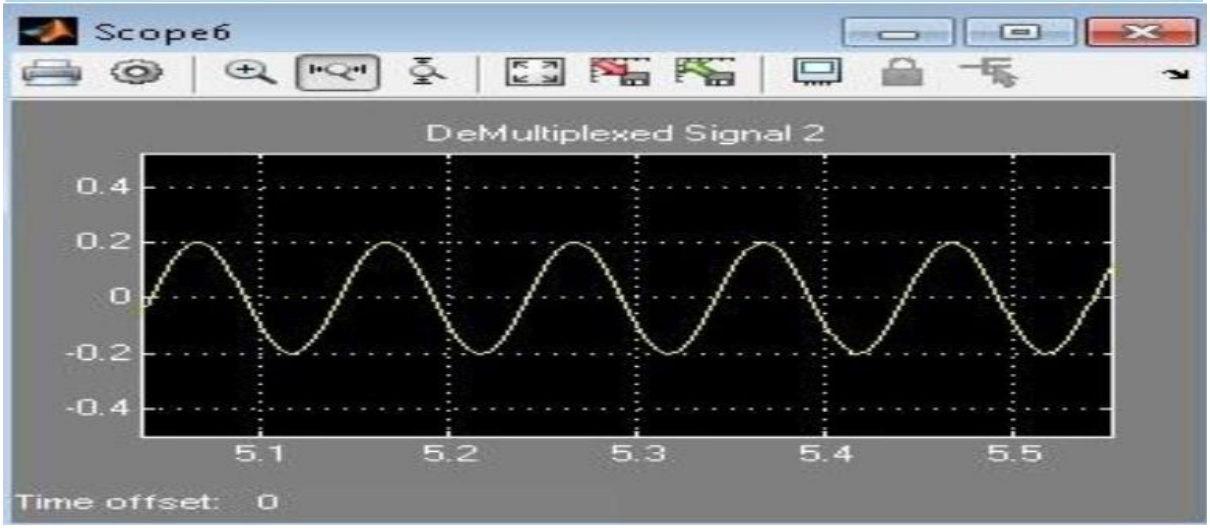


Procedure

1. Switch on the computer and click on the MATLAB icon.
2. Go to start at the bottom of the command window, then select "Simulink" then go to library browser and drag it into creating file. (or) Once you open the Matlab then click on the Simulink icon . Go to file and select new and then select model. You will get a new window.
3. Arrange the functional blocks as shown in Simulink model.
4. Assign required parameters to each functional block.
5. Observe the outputs on scope.







RESULT:

Thus the two signals are transmitted using TDM and they are demultiplexed.

4. PULSE CODE MODULATION

AIM:

Write a MATLAB program to generate PCM signal

PROGRAM:

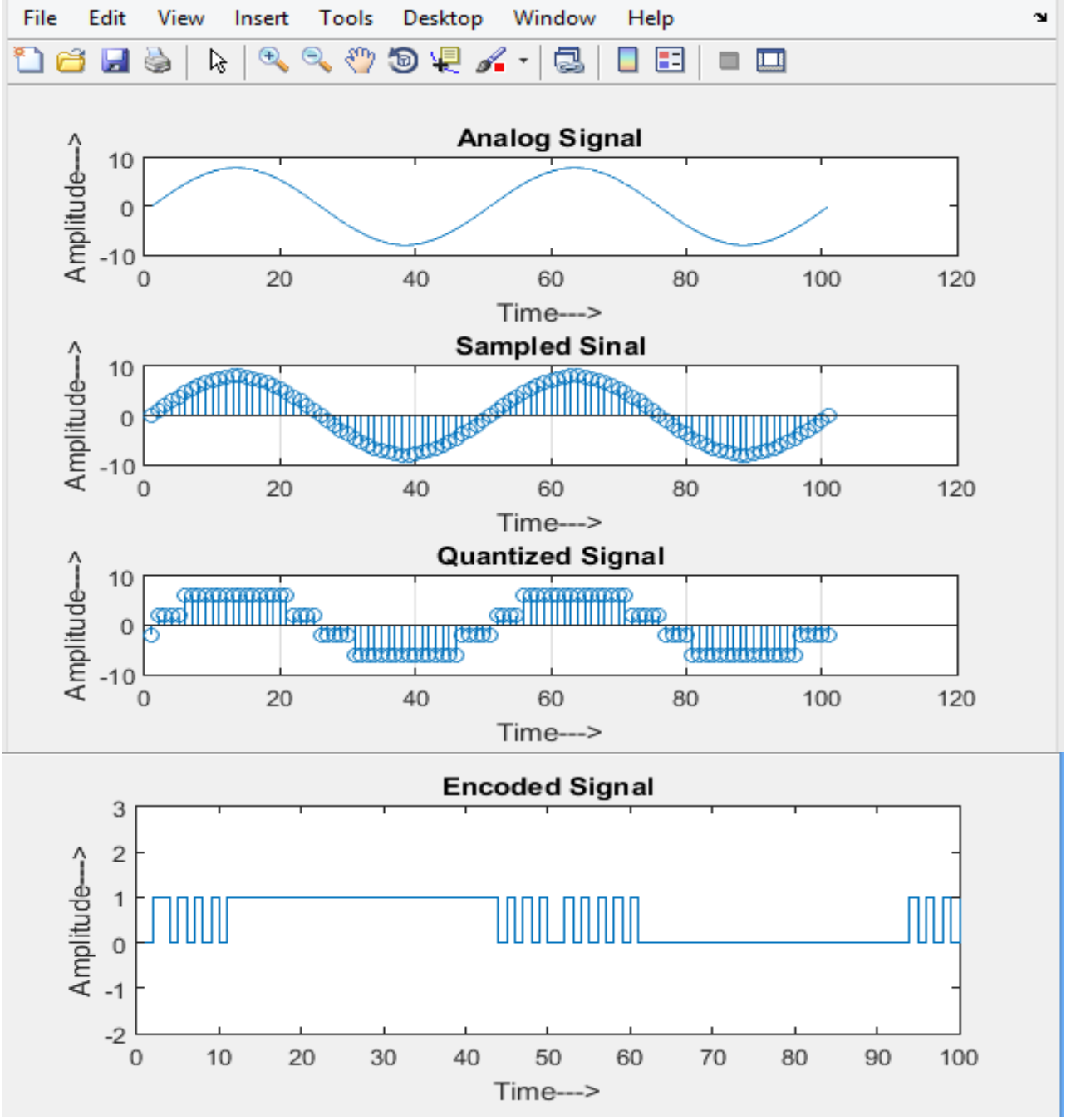
```
clc;
close all;
clear all;
n=input('Enter n value for n-bit PCM system :  ');
n1=input('Enter number of samples in a period : ');
L=2^n;

% % Signal Generation
% x=0:1/100:4*pi;
% y=8*sin(x);
% subplot(2,2,1);
% plot(x,y);grid on;
% Sampling Operation
x=0:2*pi/n1:4*pi;
s=8*sin(x);
subplot(3,1,1);
plot(s);
title('Analog Signal');
ylabel('Amplitude--->');
xlabel('Time--->');
subplot(3,1,2);
stem(s);grid on;  title('Sampled Signal');
ylabel('Amplitude--->');
 xlabel('Time--->');
vmax=8;
 vmin=-vmax;
 del=(vmax-vmin)/L;
 part=vmin:del:vmax;
 code=vmin-(del/2):del:vmax+(del/2);
 [ind,q]=quantiz(s,part,code);
 l1=length(ind);
 l2=length(q);
 for i=1:l1
    if(ind(i)~=0)
       ind(i)=ind(i)-1;
    end
%     i=i+1;
 end
  for i=1:l2
     if(q(i)==vmin-(del/2))
```

```
        q(i)=vmin+(del/2);
    end
 end
 subplot(3,1,3);
 stem(q);grid on;
 title('Quantized Signal');
 ylabel('Amplitude--->');
 xlabel('Time--->');
 %  Encoding Process
 figure
 code=de2bi(ind,'left-msb');
 k=1;
for i=1:l1
   for j=1:n
      coded(k)=code(i,j);
      j=j+1;
      k=k+1;
   end
   i=i+1;
end
 subplot(2,1,1); grid on;
 stairs(coded);
axis([0 100 -2 3]);  title('Encoded Signal');
 ylabel('Amplitude--->');
 xlabel('Time--->');
```

procedure:

1. Run MATLAB
2. Open a new script file
3. Write the code for mu-law Companding technique.
4. Run the code for execution and obtain the necessary results

Observations:



Result:

pulse code modulation is performed using MATLAB

VIVA QUESTIONS:

1. What is meant by multiplexing technique and what are the different types of Multiplexers?
2. Briefly explain about TDM&FDM?
3. What is the transmission band width of a PAM/TDM signal?
4. Define crosstalk effect in PAM/TDM system?
5. What are the advantages of TDM system?
6. What are major differences between TDM&FDM?
7. Give the value of Ts in TDM system?
8. What are the applications of TDM system and give some example?
9. What is meant by signal overlapping?
10. Which type of modulation technique will be used in TDM?

5. COMPANDING

Aim: To implement Companding (mu-law) using MATLAB

Experimental requirements: PC loaded with MATLAB software

Theory: **companding**(occasionally called **compansion**) is a method of mitigating the detrimental effects of a channel with limited dynamic range. The name is a portmanteau of**compressing** and ex**panding**.

While the compression used in audio recording and the like depends on a variable-gain amplifier, and so is a locally linear process (linear for short regions, but not globally), companding is non-linear and takes place in the same way at all points in time. The dynamic range of a signal is compressed before transmission and is expanded to the original value at the receiver.

The electronic circuit that does this is called a **compandor** and works by compressing or expanding the dynamic range of an analog electronic signal such as sound. One variety is a triplet of amplifiers: a logarithmic amplifier, followed by a variable-gain linear amplifier and an exponential amplifier. Such a triplet has the property that its output voltage is proportional to the input voltage raised to an adjustable power. Compandors are used in concert audio systems and in some noise reduction schemes such as dbx and Dolby NR (all versions).

Procedure:

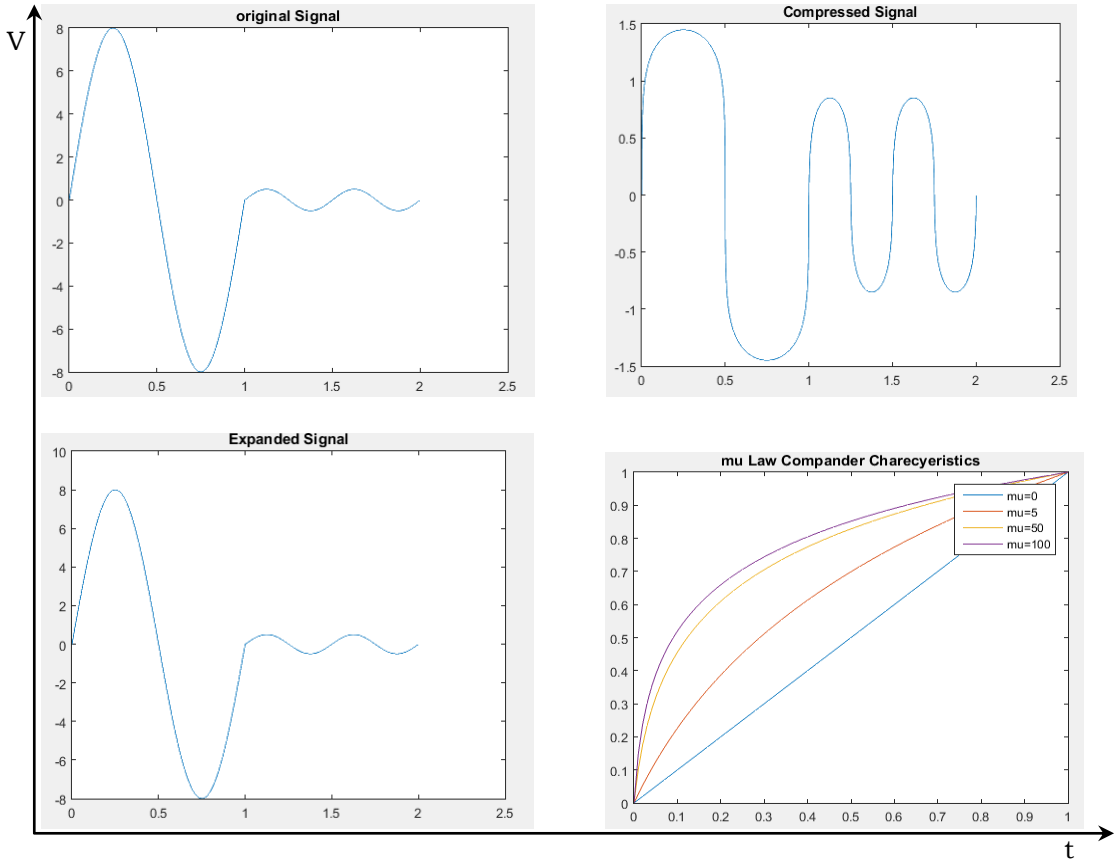
1. Run MATLAB
2. Open a new script file
3. Write the code for mu-law Companding technique.
4. Run the code for execution and obtain the necessary results

Program:

```
clc
clear
close all
fm=1;
A1=8;
A2=0.5;
Ts=1/(1000*fm);
t=0:Ts:1;
Signal1=A1*sin(2*pi*fm*t);
Signal2=A2*sin(2*pi*2*fm*t);
Signal=[Signal1 Signal2];
t1=0:Ts:2+Ts;
plot(t1,Signal)
title('original Signal')
mu=100;
Norm_Signal=(1/max(Signal))*Signal;
Signal_compress=(log(1+mu*abs(Signal))./log(1+mu)).*sign(Signal);
figure, plot(t1,Signal_compress);
title('Compressed Signal')
Signal_Expand=(1/mu)*(((1+mu).^abs(Signal_compress))-1).*sign(Signal_compress);
figure,plot(t1,Signal_Expand)
title('Expanded Signal')
```

```
mu=[0 5  50 100];
Rand_signal=0:0.01:1;
figure,
for i=1:length(mu)
   if mu(i)==0
      Rand_Signal_compress=Rand_signal;
      plot(Rand_signal,Rand_Signal_compress)
      hold on
   else

Rand_Signal_compress=((log(1+(mu(i)*abs(Rand_signal))))./(log(1+mu(i)))).*sign(Rand_si
gnal);
       plot(Rand_signal,Rand_Signal_compress)
       hold on
   end
end
legend('mu=0','mu=5','mu=50','mu=100');
title('mu Law Compander Charecyeristics')
a=max(abs(Rand_Signal_compress));
```

Observations:



RESULT:

Companding is performed using MATLAB

VIVA QUESTIONS:

1. Define Companding?
2. What is the principle of companding?
3. What is the main advantage of companding?
4. Explain μ-law and A-law companding characteristics?